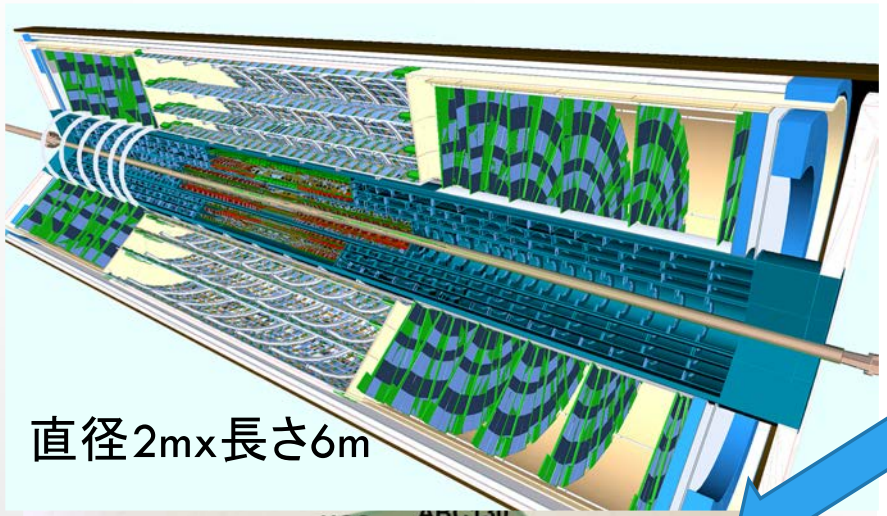
新型半導体検出器の開発

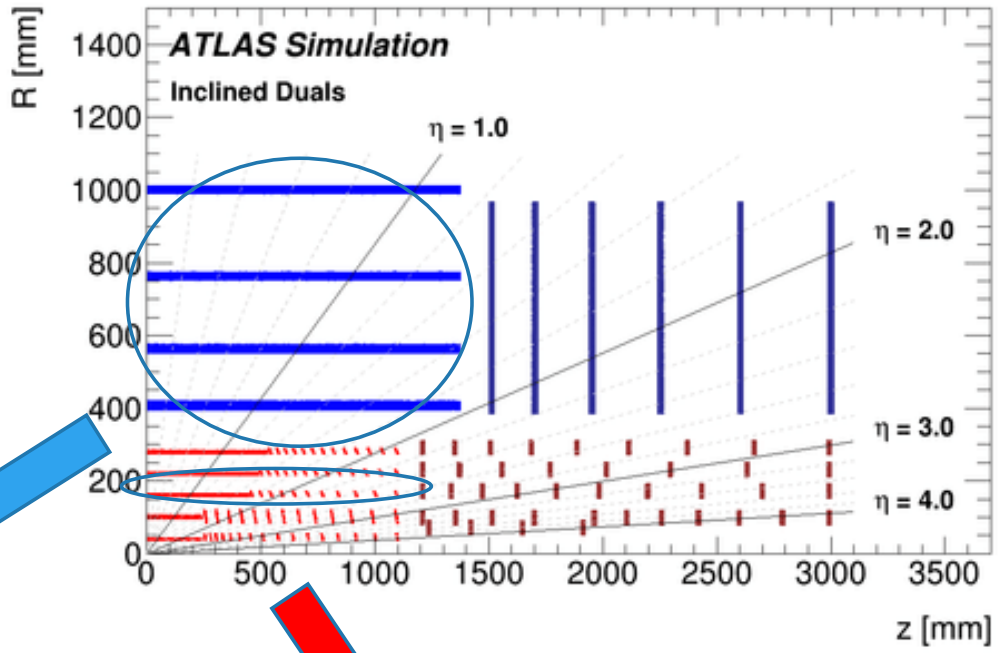
原　和彦

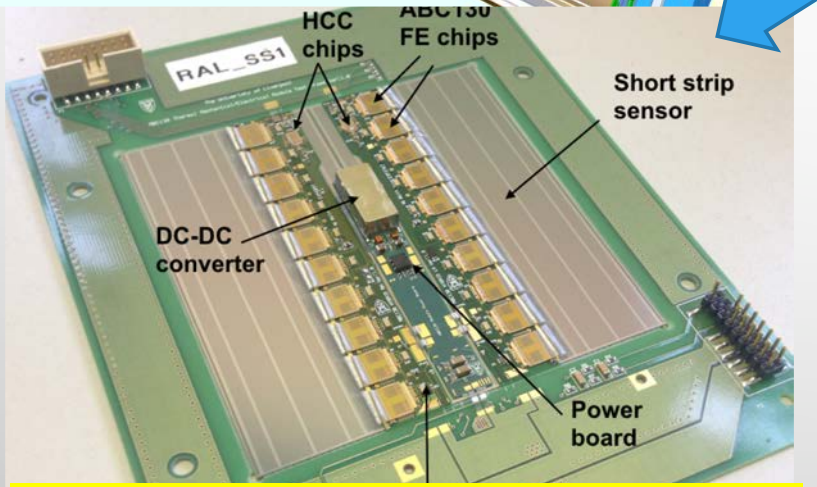
光量子計測器開発部門

新型半導体検出器

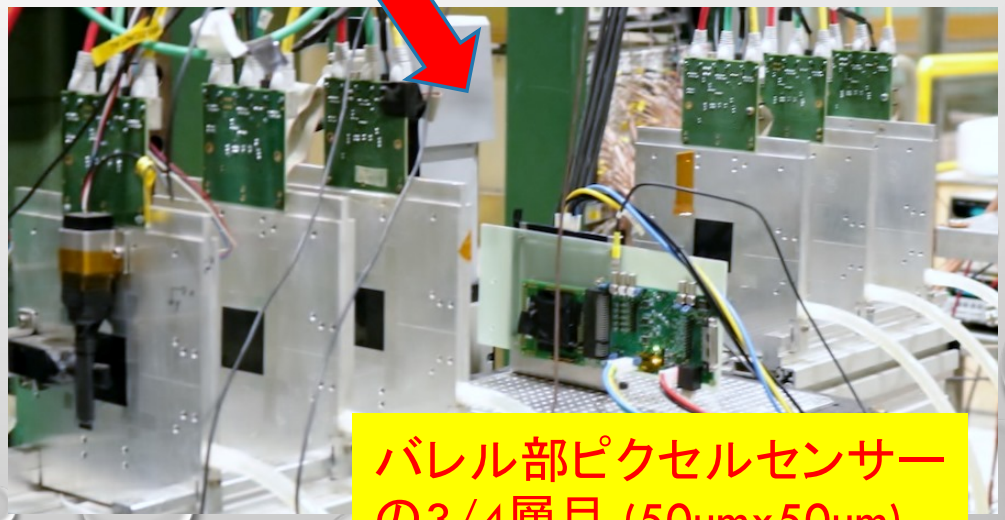
- 高輝度LHC(HL-LHC, 2023~)のための検出器開発







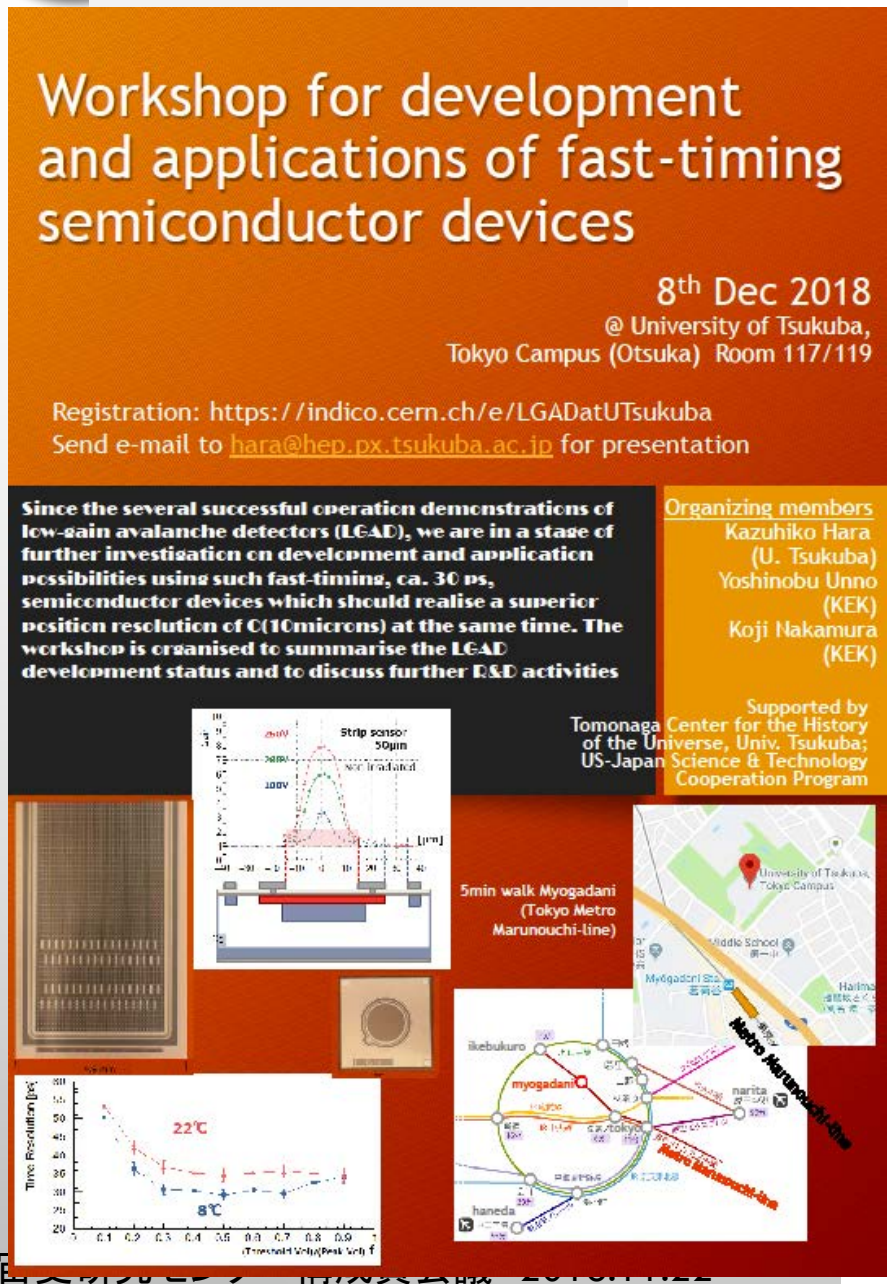
バレル部ストリップセンサーの半数
(75.5umx2.4/4.8cm)



バレル部ピクセルセンサーの3/4層目 (50umx50um)

新型半導体検出器

❑ 高時間分解能LGAD



Workshop for development and applications of fast-timing semiconductor devices

8th Dec, 2018

@University of Tsukuba, Tokyo Campus 117/119

Tentative Program(Nov.12, updated)

Room 117

9:50-10:00 Kazuhiko Hara (U Tsukuba)
Welcome and Introduction

10:00-10:20 Kyoji Onaru (U Tsukuba)
Performance Evaluation of HPK Segmented LGAD

10:25-10:50 Sayaka Wada (U Tsukuba)
Timing results of HPK LGAD PD

11:00-11:20 Ryosuke Mori (Kyushu U)
Development of inverse-LGAD for PID application in ILC

11:30-11:50 Taiga Yamaya (NIRS, QST)
Radiation detectors for positron emission tomography

<working lunch: bento> Room move to 119

12:00-12:20 Daiki Hayakawa (U Genève)
Development of fast, monolithic silicon pixel sensors in a SiGe Bi-CMOS process for TOF-PET

12:30-12:50 Sayaka Wada (U Tsukuba)
TCAD simulation of LGAD

13:00-13:20 Adriano Lai (U di Cagliari)
3D fast timing sensors and related electronics

13:30-13:50 Masahiko Saito (U Tokyo)
Tracking at FCC

14:00-14:20 Simon Mezza (UCSC)
LGAD Development for ATLAS HGTD

14:30-14:50

15:00-15:20 Koji Nakamura (KEK)
Summary and Prospects

By 16:00 Adjourn

新型半導体検出器

- 読出し回路一体型ピクセル検出器SOI

"MGM Beach Resorts" in **Chennai, India**.
https://indico.cern.ch/event/710050/

International Advisory Committee

Marina Artuso, Syracuse University
Gian Mario Bilei, INFN Perugia
Daniela Bortoletto, University of Oxford
Richard Brenner, Uppsala University
Davis Christian, Fermilab
Paula Collins, CERN
Zdenek Dolezal, Charles University in Prague
Lars Eklund, University of Glasgow
Francesco Forti, University of Pisa and INFN Pisa
Kazuhiko Hara, University of Tsukuba
Roland Horisberger, PSI
Manfred Kramer, CERN
Hans-Guenther Moser, Max Plank Institute for Physics, Munich
Hwanbae Park, Kyungpook University
Chris Parkes, University of Manchester
Sally Seidel, University of New Mexico

Development of SOI Monolithic Pixel Detector for Fine Measurement of Space and Time SOFIST

K. Hara (Univ. Tsukuba)
for SOIPIX Collaboration

筑波大学
University of Tsukuba

SOIPIX
Silicon-On-Insulator Pixel Detector Project

SOFIST development:
U. Tsukuba: K. Hara, D. Yamauchi, R. Abe, S. Iwanami, H. Murayama, K. Watanabe
KEK: T. Tsuboyama, M. Yamada, S. Ono, Y. Arai, Y. Ikegami, I. Kurachi, M. Togawa, J. Haba
Tohoku U.: Li. Taohan

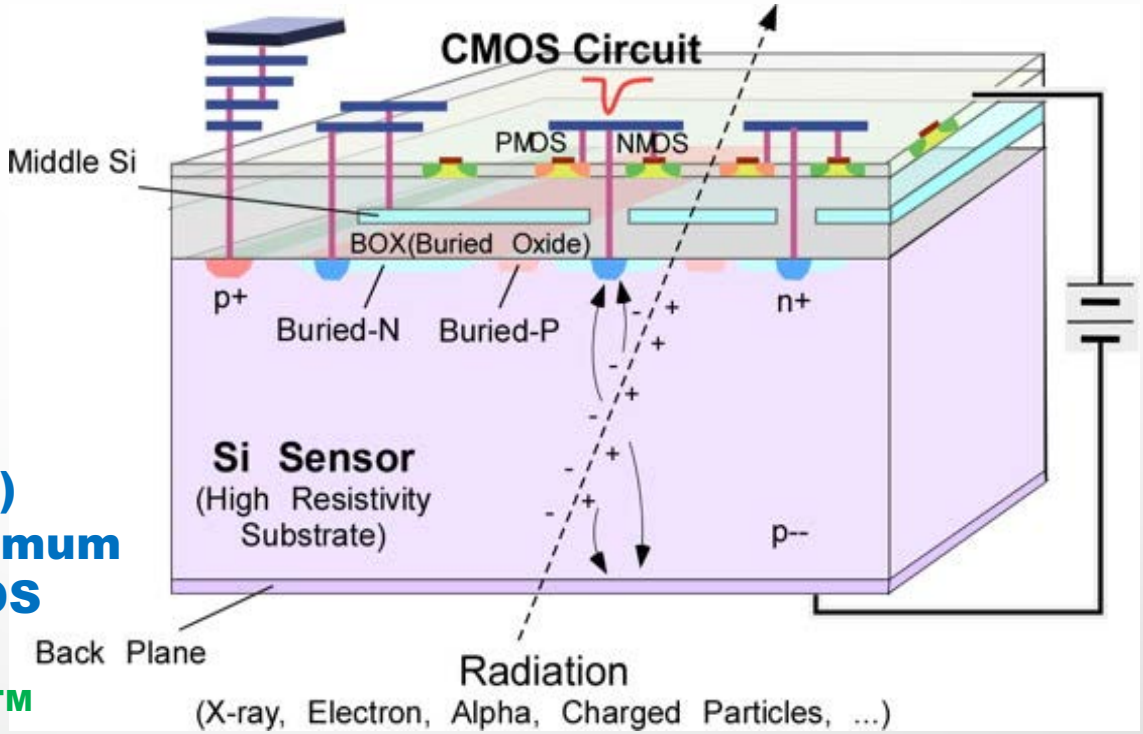
Project supported by
JSPS Grant-in-Aid for Scientific Research on Innovative Areas (2013-2017)

OUTLINE

1. SOI PIXEL Sensor Development - Introduction
2. Highlights from 5-Year Grant-in-Aid (summary by Y. Arai)
3. SOFIST
   - design & developments
   - SOFIST-1 position resolution
   - SOFIST-2 timestamp resolution
   - SOFIST-3 quick evaluation
4. SOFIST-4 3D stacking
5. Summary

SOI PIXEL DEVICES

SOI: SILICON-ON-INSULATOR
CMOS circuitry fabricated on buried oxide(BOX)
LAPIS 0.2um FD-SOI



Features:

- **Monolithic (no metal bumps)**
- **SOI-CMOS (FETs fully isolated)**
- **Can choose* substrate of optimum resistivity (fully depleted CMOS sensors possible)**

***SOITEC SmartCut™**

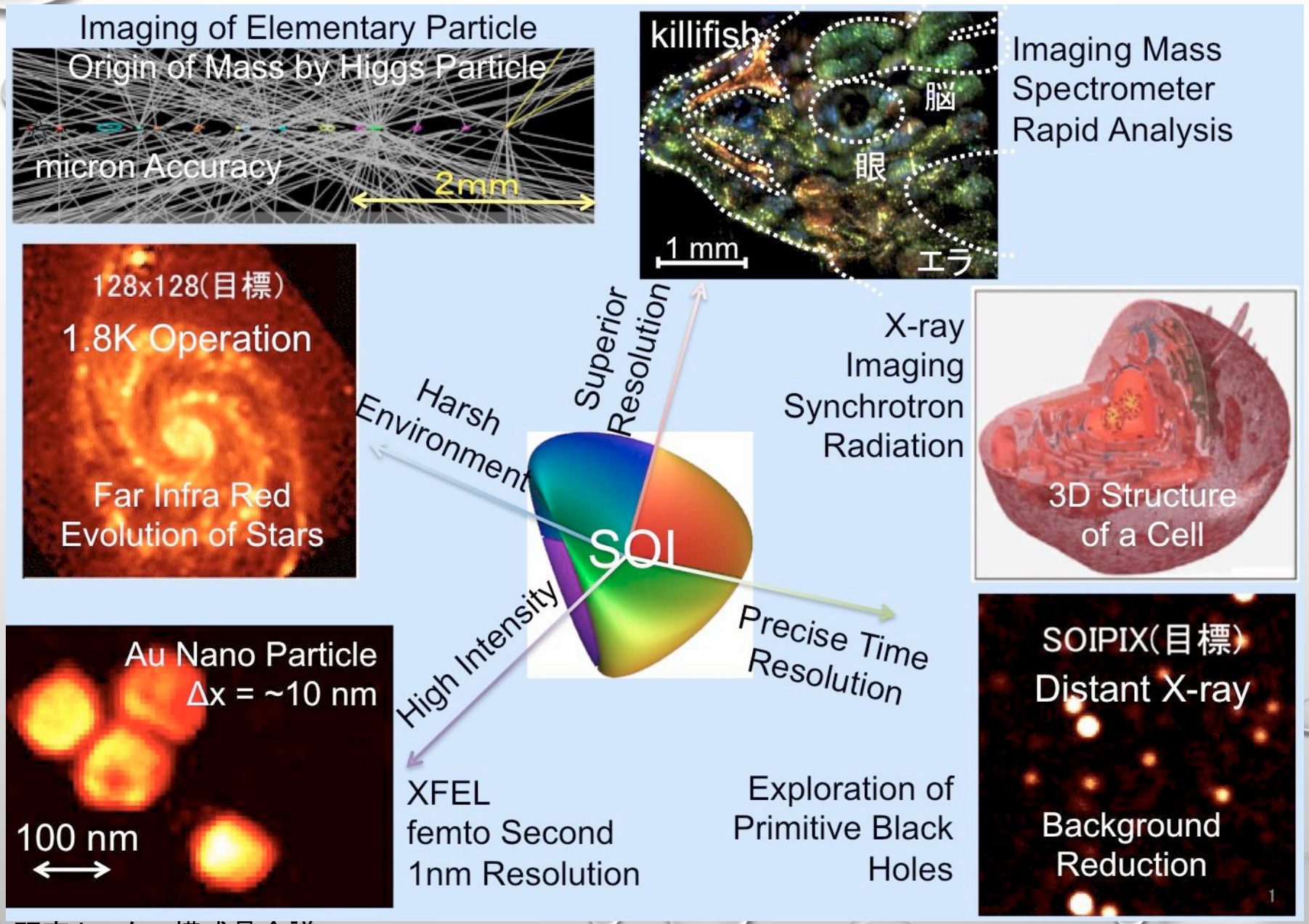
many excellent features

- **Material budget**
- **S/N**
- **power dissipation**
- **speed**
- **cost**
- **Pixel size**
- **single event effects**
- **latch up**
- **Operation temp. (0.3K～570K)**

TID tolerance improved to 1MGy by introducing double SOI wafer (HSTD11)

GRANT-IN-AID (FY2013-17)

INTERDISCIPLINARY RESEARCH ON QUANTUM IMAGING OPENED WITH 3D SEMICONDUCTOR DETECTOR



第1回「量子線イメージング研究会」@京都大学　のお知らせ

The 1st Workshop on Quantum Beam Imaging

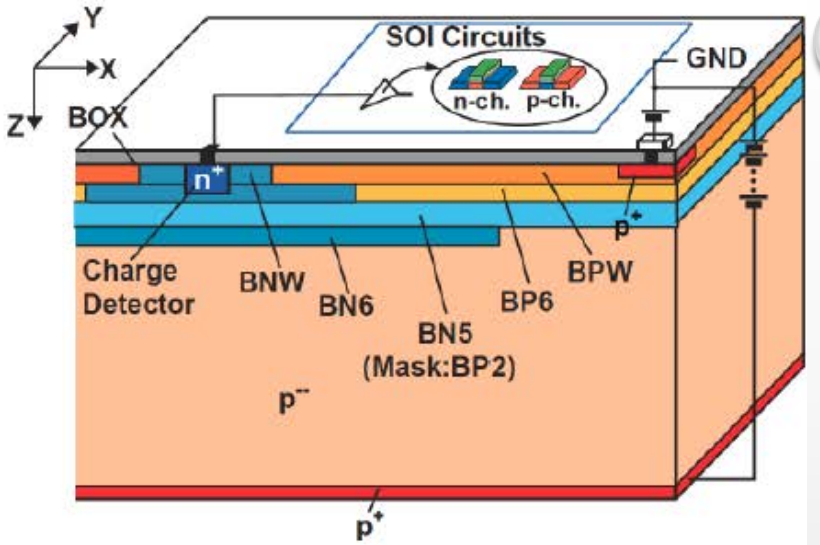
25-26 Sept 2018

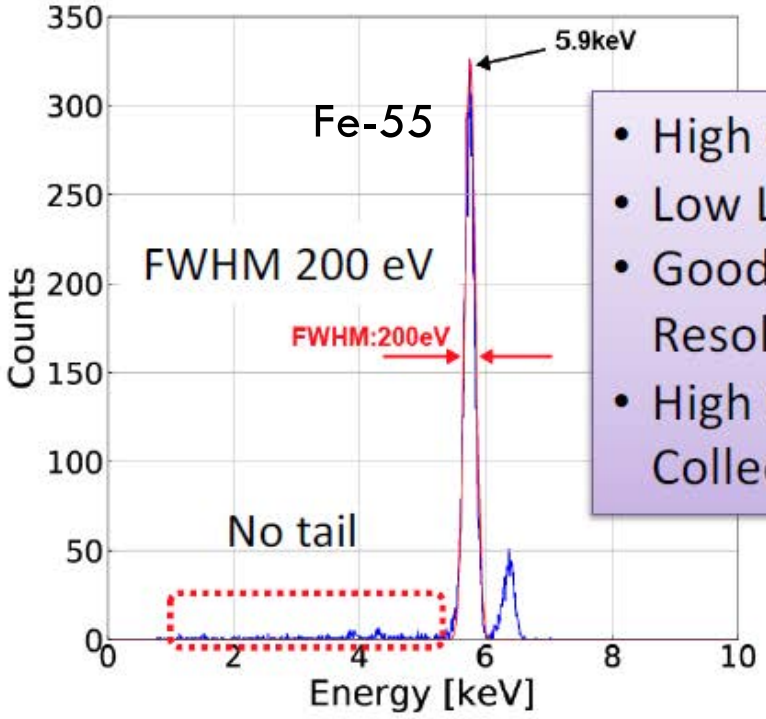
- ✓ Be ready for new application for 5-year grant-in-aid
- ✓ Establish SOI imaging sensor consortium
- ✓ SOI summary talk by Y.Arai (KEK)

HIGHLIGHT-1 (SOIPIX-PDD)

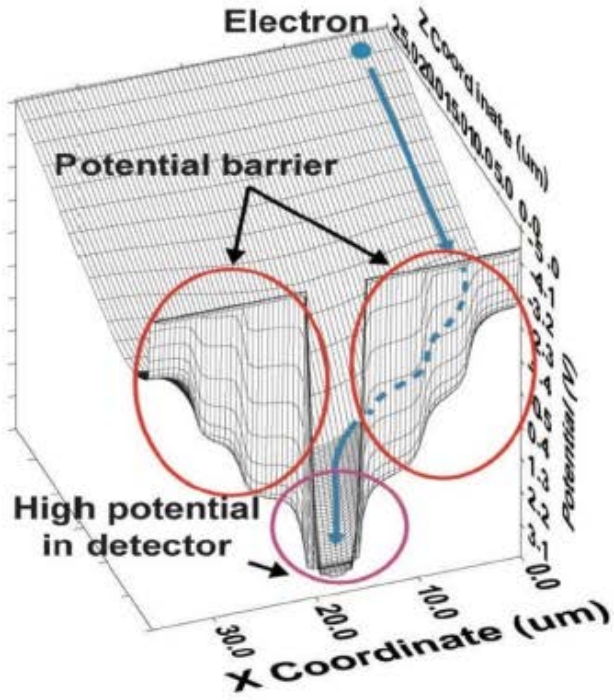
New Sensor Structure: Pinned Depleted Diode (SOIPIX-PDD)

Gain = 70 μV/e-
Noise = 11.0 e-
Dark Current = 57 pA/cm2 @-35˚C



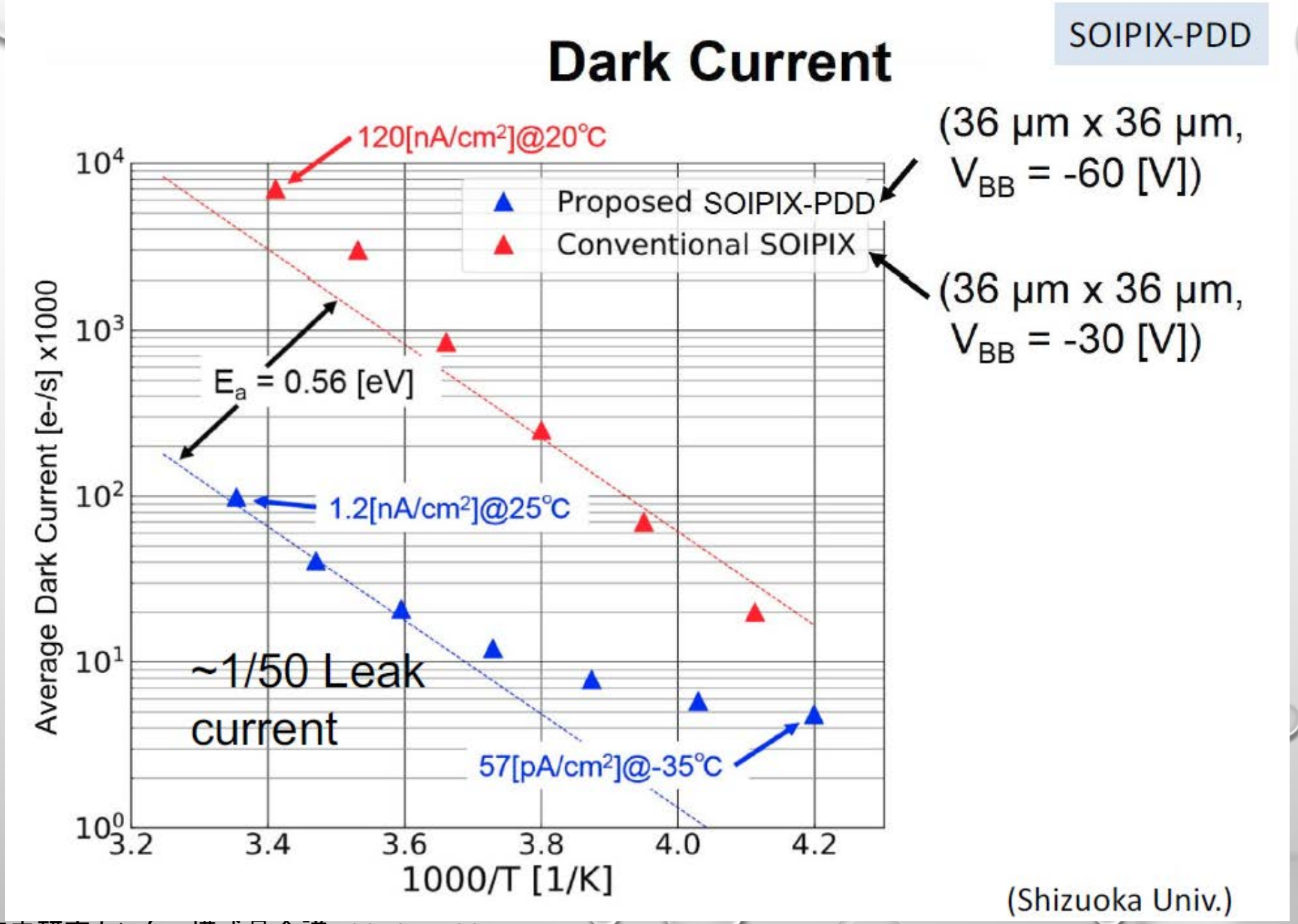


- High Gain
- Low Leak Current
- Good Energy Resolution
- High Charge Collection Efficiency



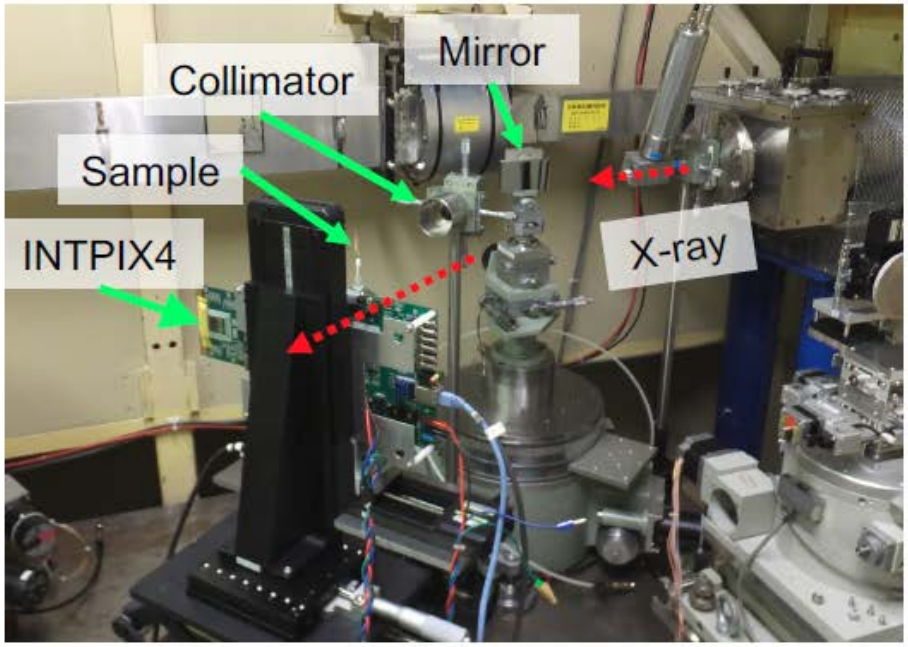
(Shizuoka U. 川人研)

HIGHLIGHT-1 (SOIPIX-PDD)

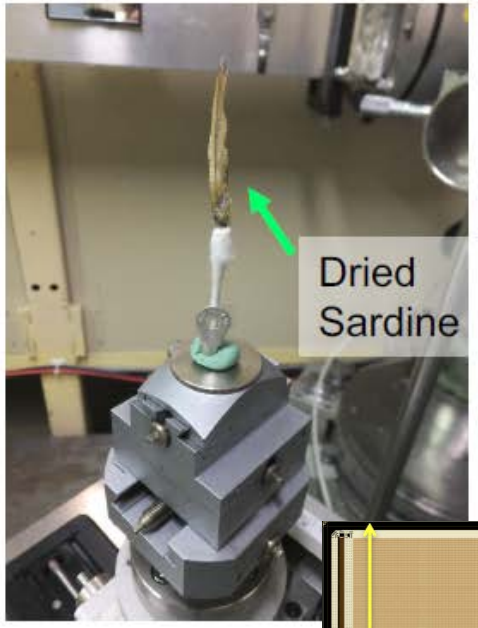


HIGHLIGHT-2 (INTPIX4)

3D CT Imaging at KEK PF

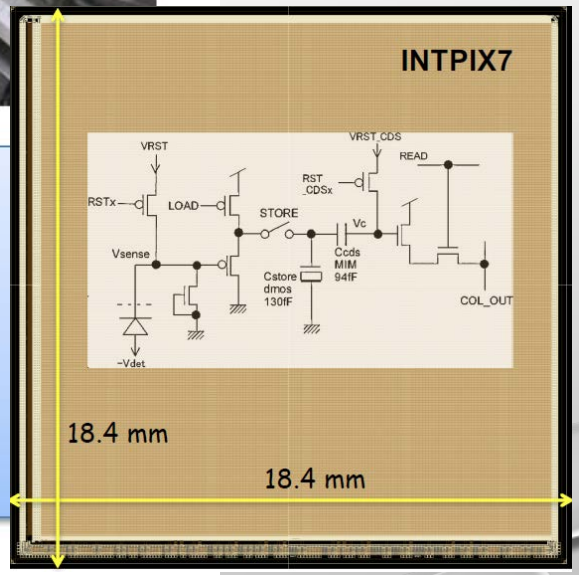


INTPIX



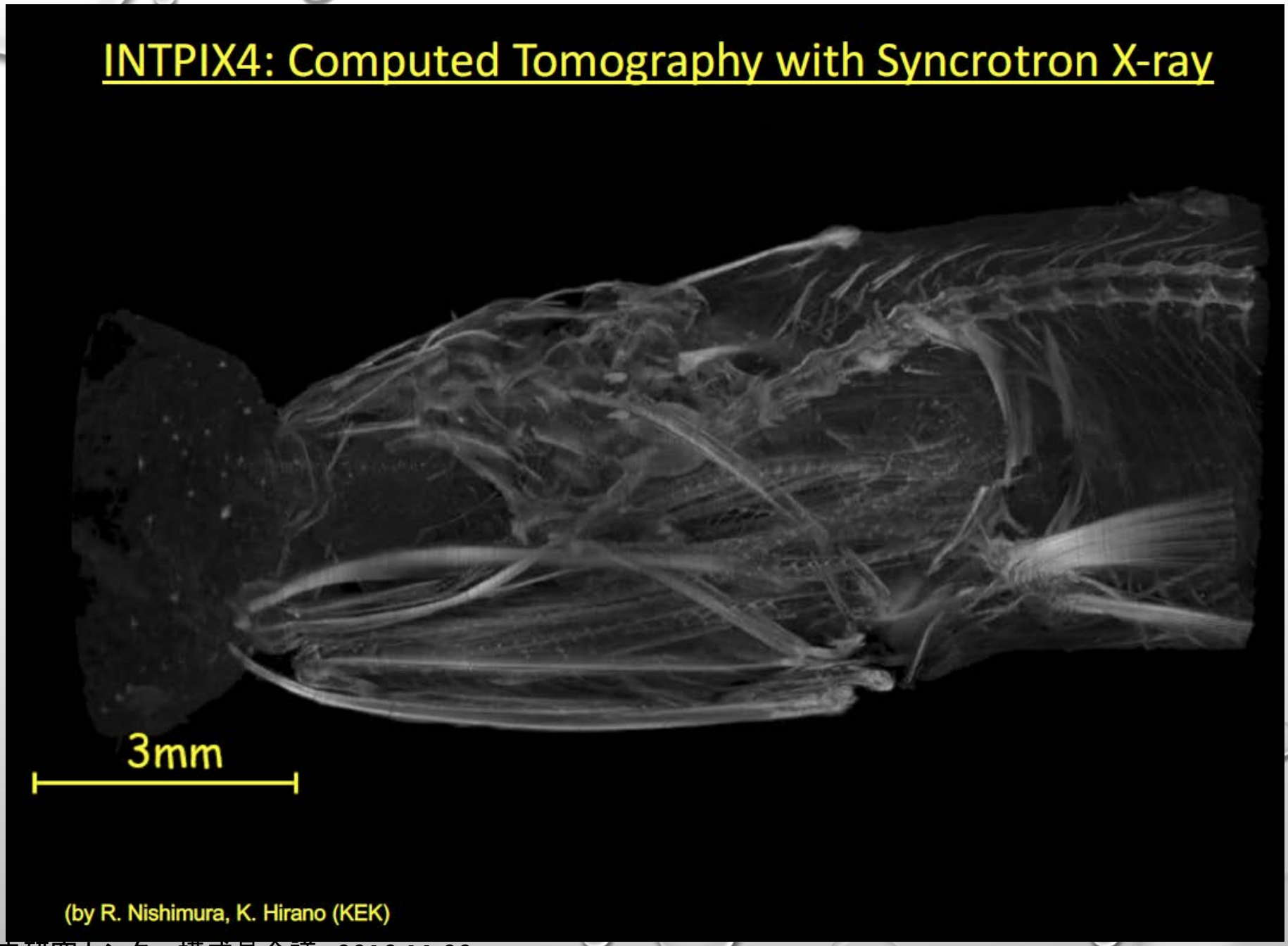
Integration
&global shutter

- Sensor : INTPIX4 FZn, Backside Illumination
- HV : 200V、Integration Time : 1ms、ScanTime : 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy : 9.5keV
- Took images for 0~180° at every 1 degree.

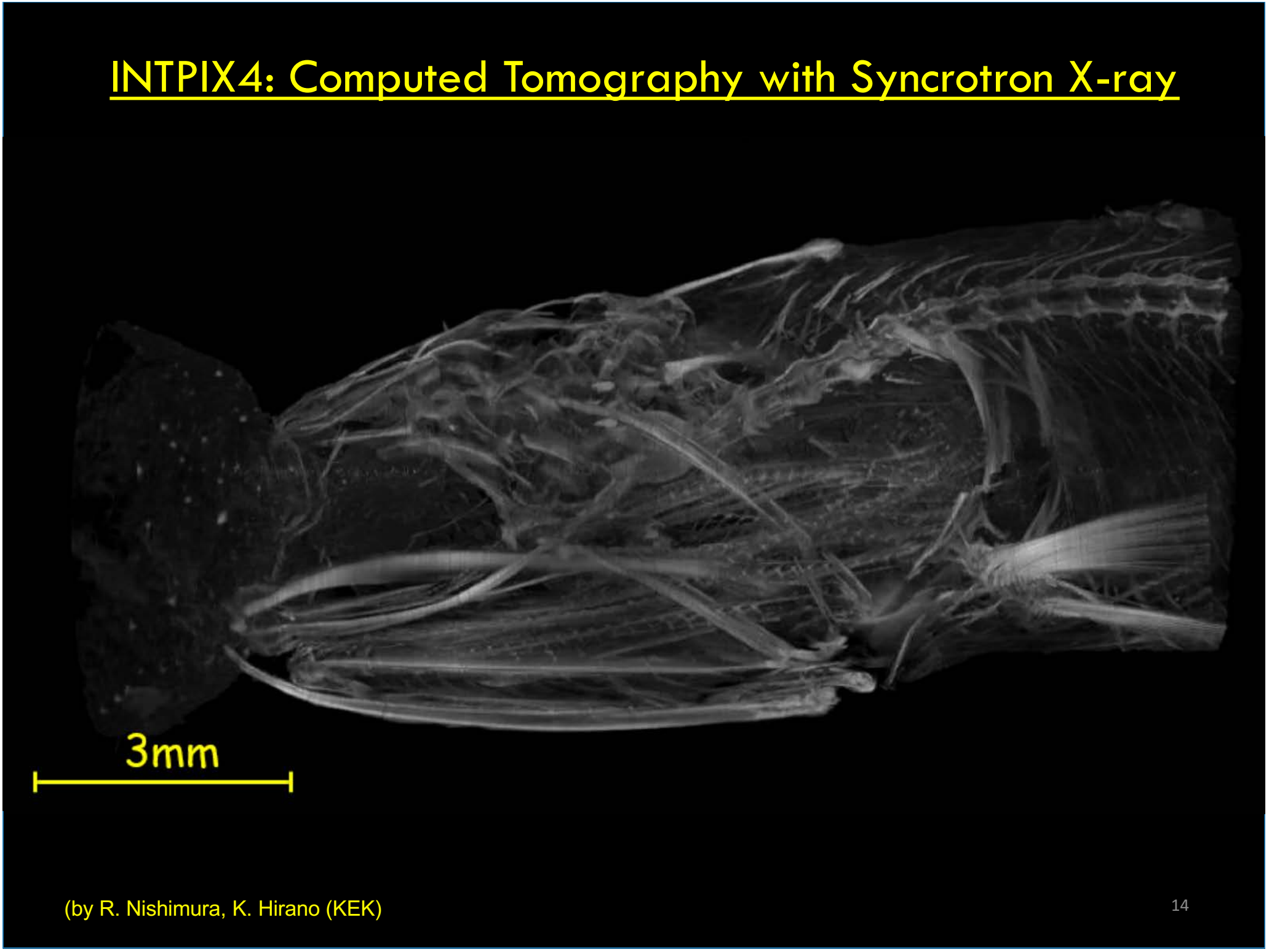


(by R. Nishimura, K. Hirano (KEK)

HIGHLIGHT-2 (INTPIX4)



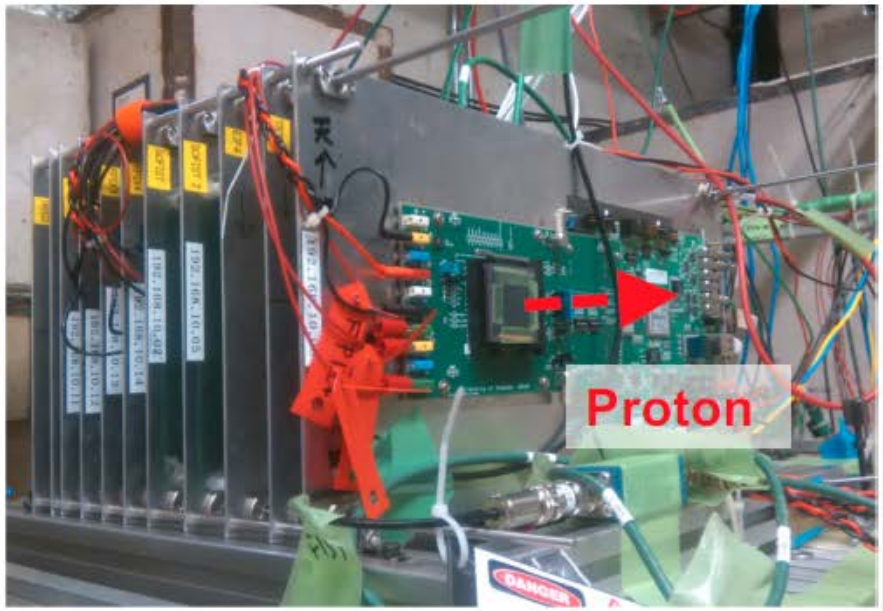
INTPIX4: Computed Tomography with Syncrotron X-ray

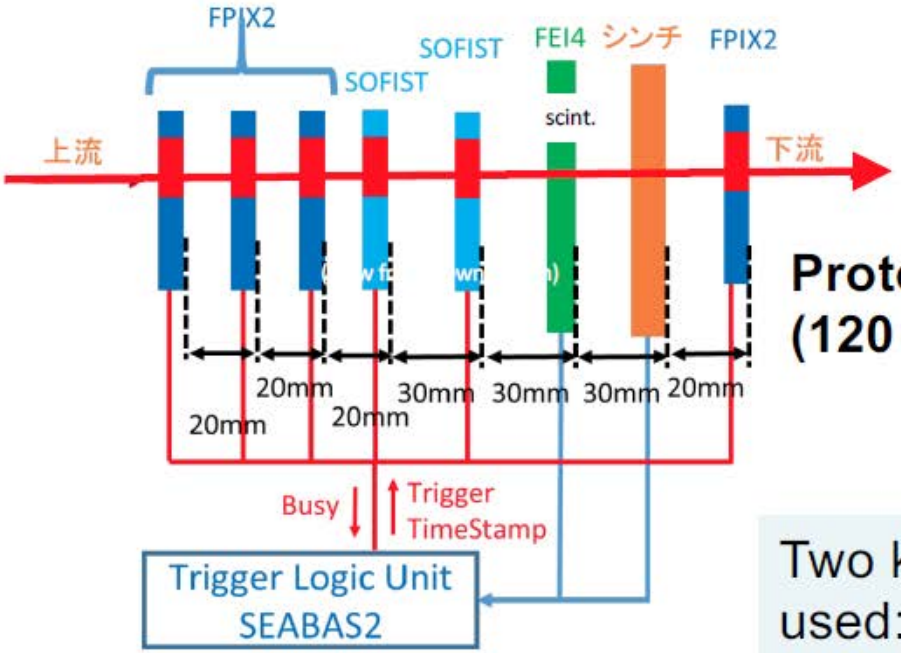


(by R. Nishimura, K. Hirano (KEK)

HIGHLIGHT-3 (FPIX2)

Tracking Resolution:
High-Energy Beam test @Fermi National Accelerator Lab.





Proton Beam (120 GeV/c)

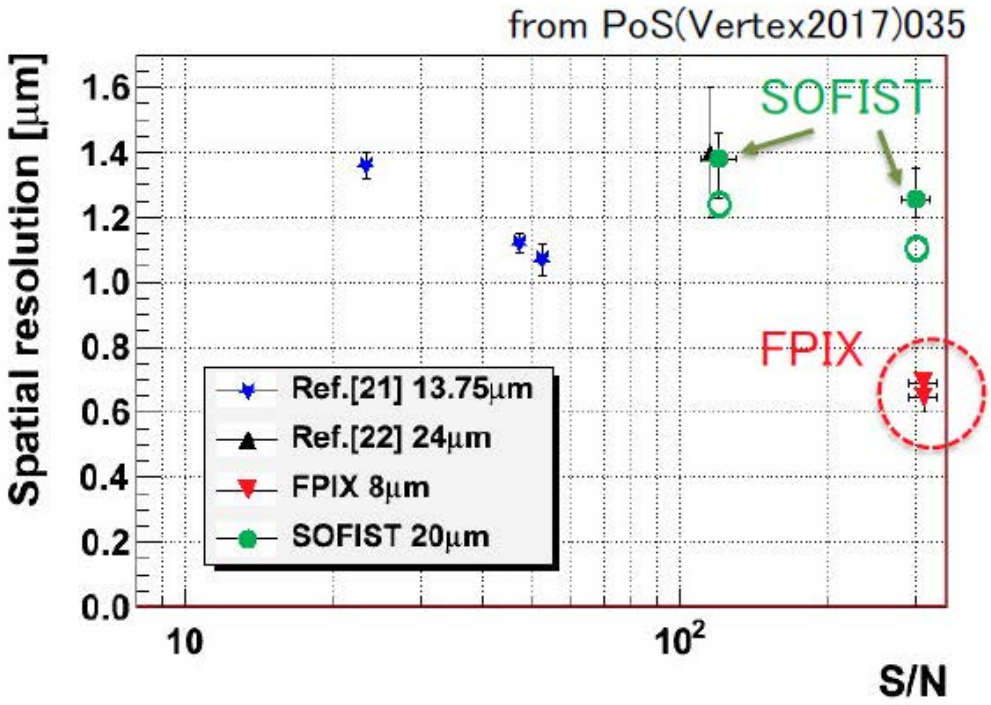
Two kinds of SOIPIX-DSOI detectors are used:

- FPIX2 x 4: 8 μm square pixel detector
- SOFIST1 x 2: 20 μm square pixel detector

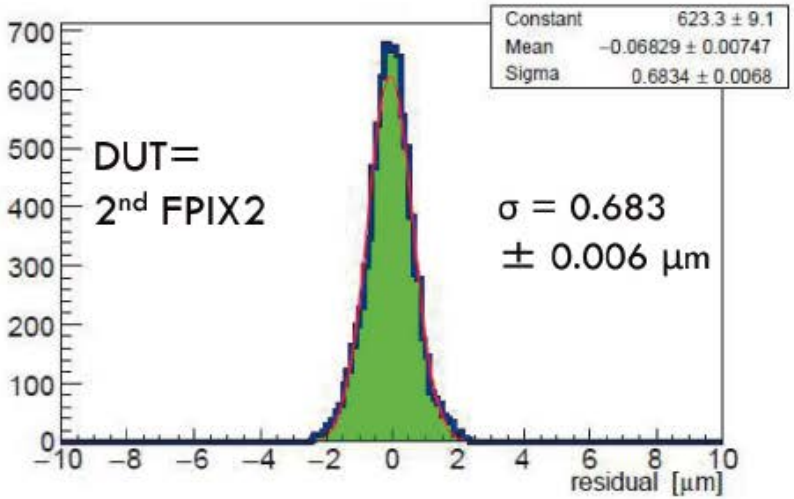
U Tsukuba/KEK

HIGHLIGHT-3 (FPIX2)

SOI Vertex Detector (FPIX、SOFIST)



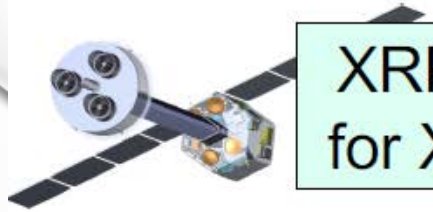
Detector	Pixel size	Resolution
ATLAS Pix	13.75 μm	1.1 μm
DEPFET	24 μm	1.4 μm
SOFIST	20 μm	1.2 μm
FPIX	8 μm	**0.65 μm**



Better than 1 μm Position Resolution for high-energy charged particle is achieved first in the world !
Concurrent Timing Measurement with 1.9 ~~1.6~~μs resolution is also performed.

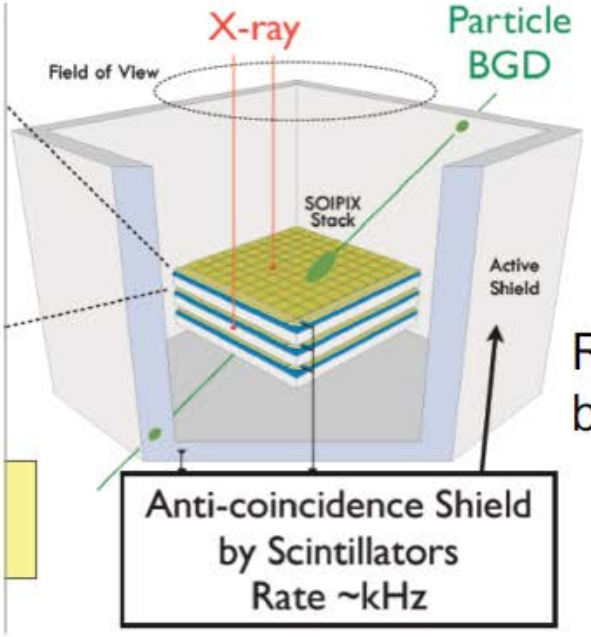
Ref.[21] ATLAS sensor, ATLAS-CONF-2013-005
Ref.[22] DEPFET detector, https://cds.cern.ch/record/1967037

HIGHLIGHT-4 (XRPIX5)



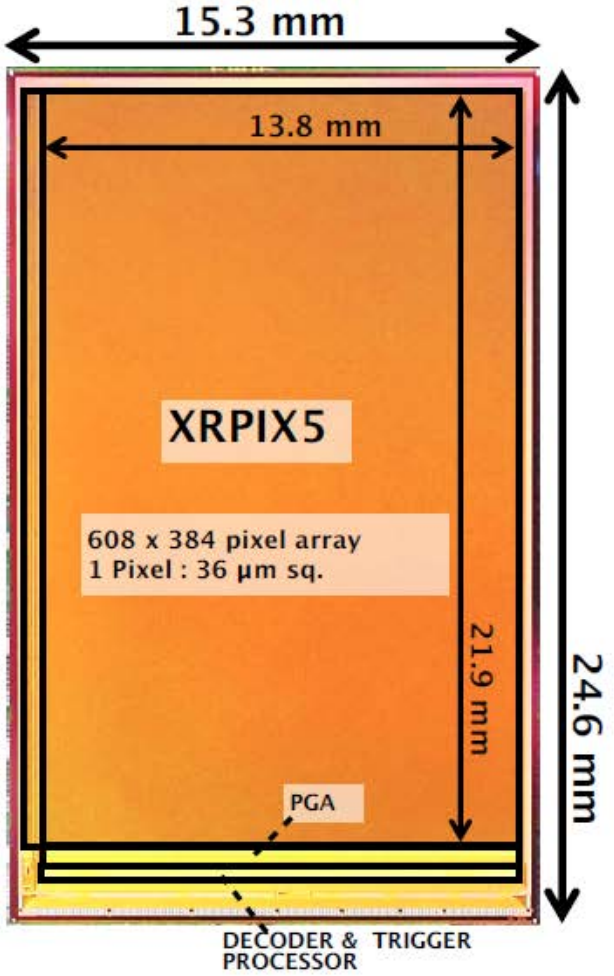
XRPIX: Event-Driven Detector for X-ray Astronomical Satellite

Timing resolution of CCD is too poor to make anti-coincidence.



Prompt hit signal generation

Remove cosmic-ray back ground.

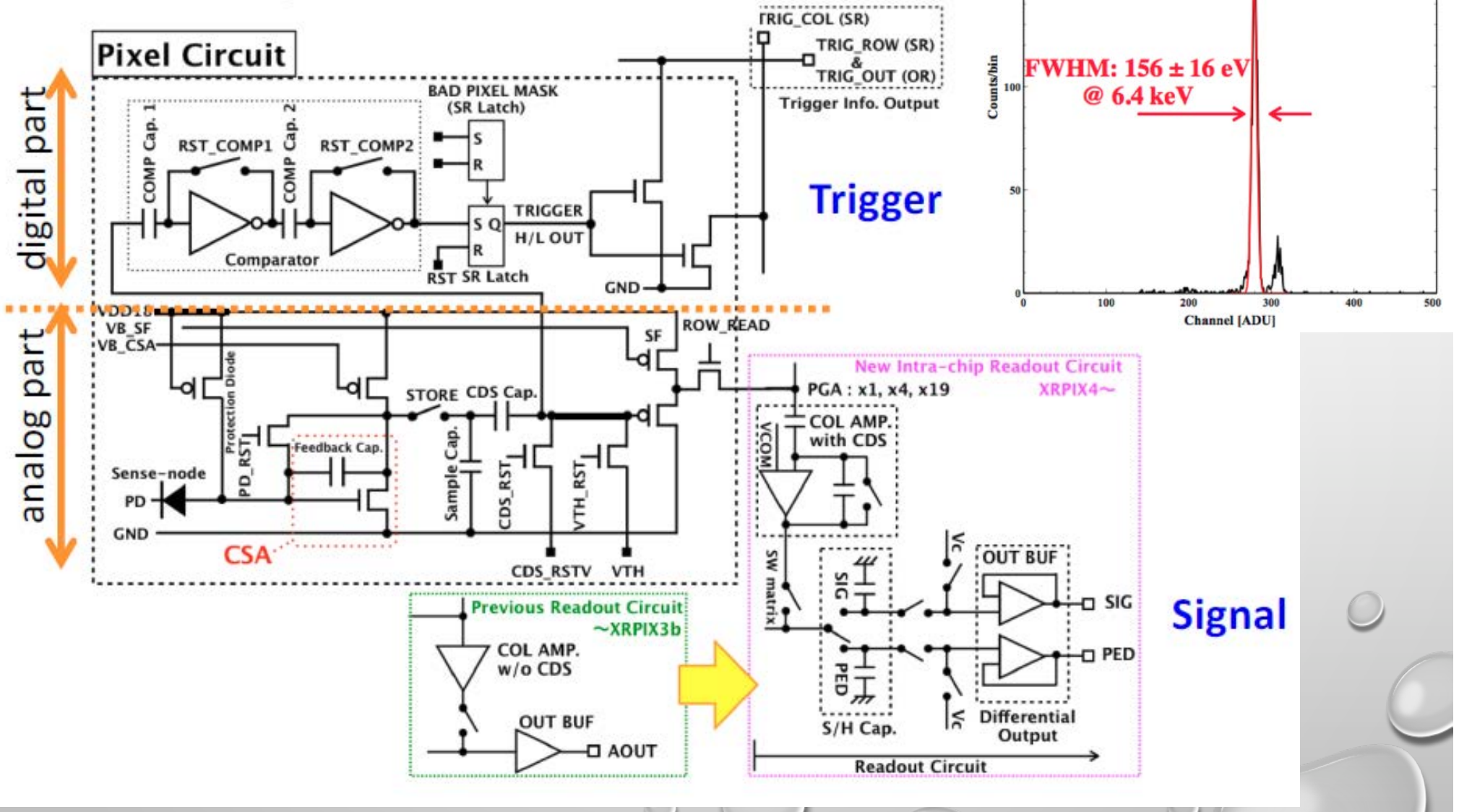


Aiming to install in the next satellite FORCE (Forcusing On Relativistic universe and Cosmic Evolution)

(Kyoto U. etc.)

HIGHLIGHT-4 (XRPIX5)

XRPIX: Event Driven X-ray Astronomy Detector



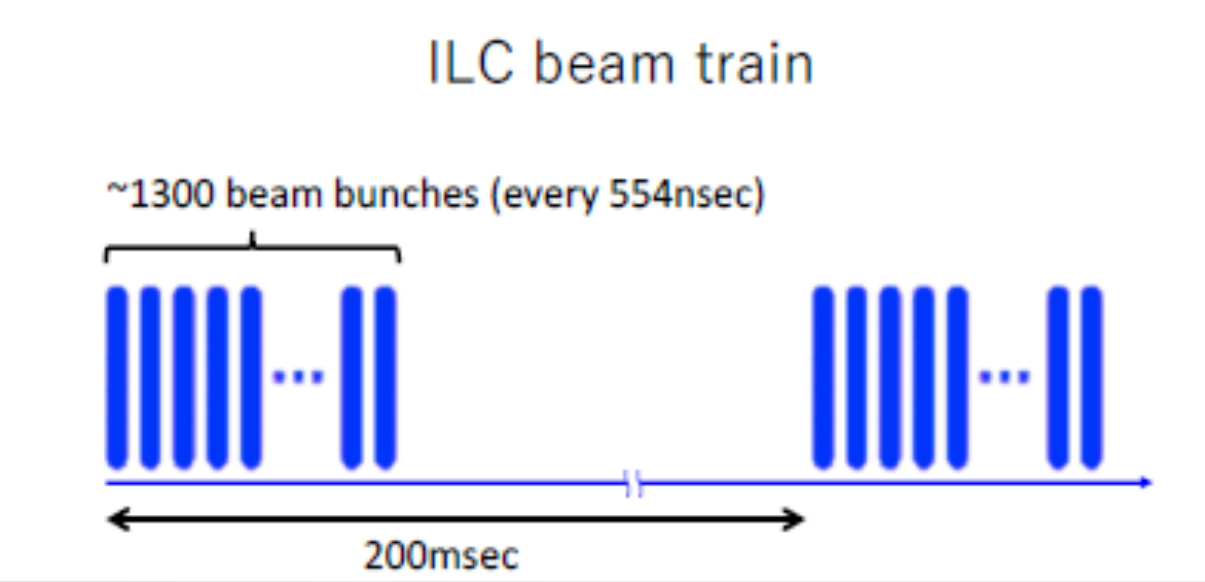
HIGHLIGHT-4 (XRPIX5)

	Hitomi CCD	eROSITA pnCCD	XRPIX
Pixel Size	24 μ m	75 μ m	36 μ m
No. of Pixel	1200 x 1200	384 x 384	608 x 384
Depletion Thickness	200 μ m	450 μ m	300 μ m
Energy Resolution (@6.4keV)	165eV	150eV 149eV/FWHM	156eV (Test Chip、1 pix)
Timing Resolution	4 sec	50 msec 20us→2~4us/line	→ 10 μsec x5000 fast !
Anti Coincidence	X	X	O
Operating Temp.	−120℃	−95℃	−20℃

Energy resolution as good as CCD's
Much faster!
Muon veto possible

SOFIST SOI MONOLITHIC PIXEL DETECTOR FOR FINE MEASUREMENT OF SPACE AND TIME

Allows time and space point measurement
Design specified to meet the requirements for the ILC experiment



Main requirements:

- Position resolution <3um
- Low material <0.2%Xo/layer
- TID~1kGy/year
- NIEL ~$10^{11} n_{eq}/cm^2$/year

Readout between trains
bunch ID highly preferred
Power dissipation: <50mW/cm^2

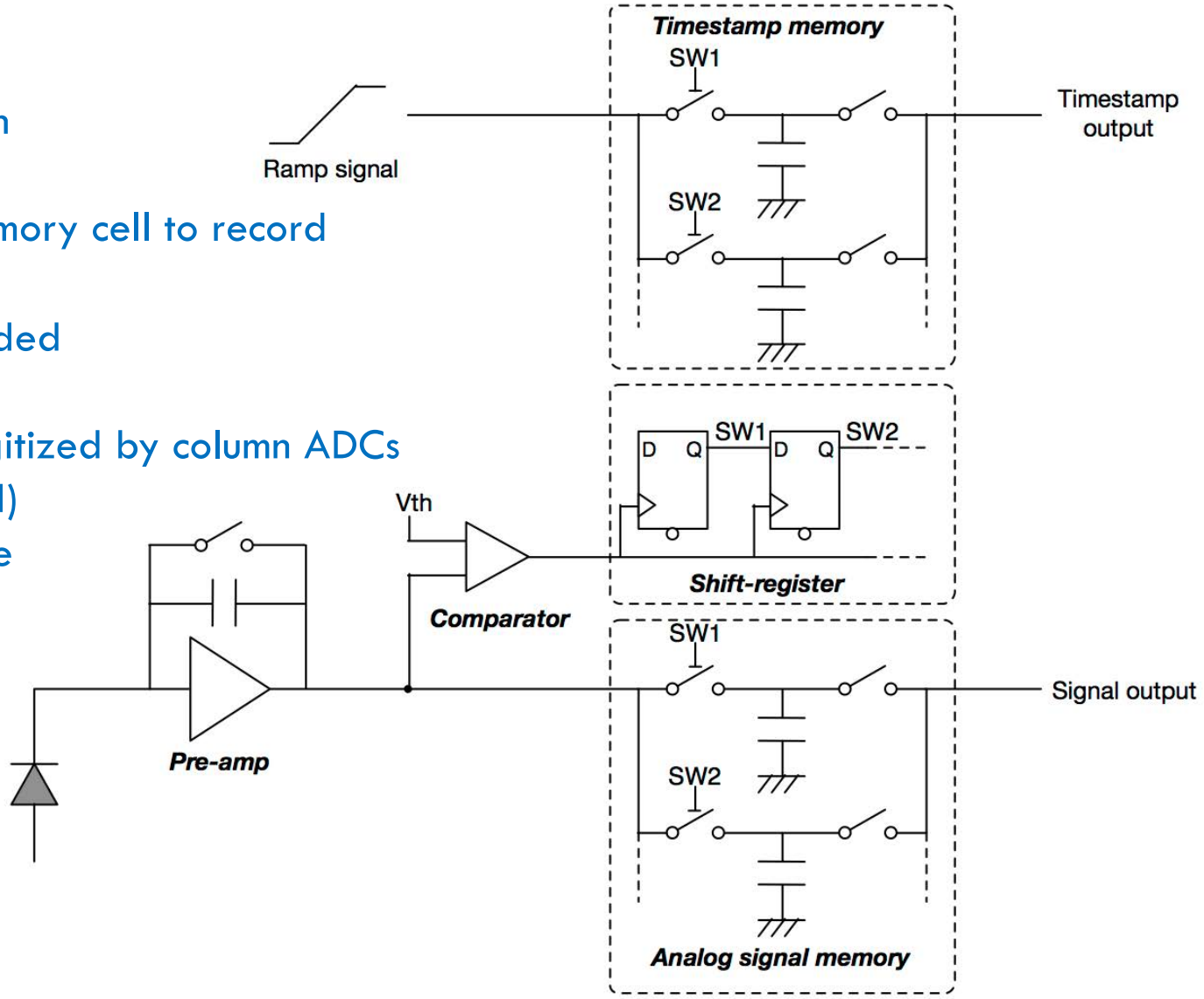
The goal is a sensor with both good spatial resolution of <3um and time resolution <1us.

- ✓ pixel size ~20um-sq with analog readout
- ✓ timestamp recording the ramping voltage
- ✓ store the data allowing multiple hits on the same pixel
- ✓ on-chip ADCs &zero-suppression for fast data transfer

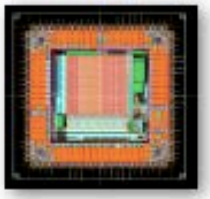
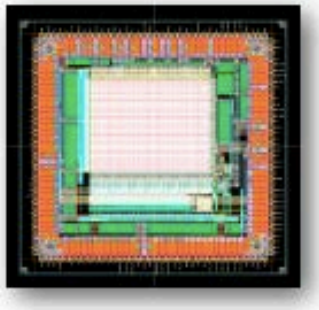
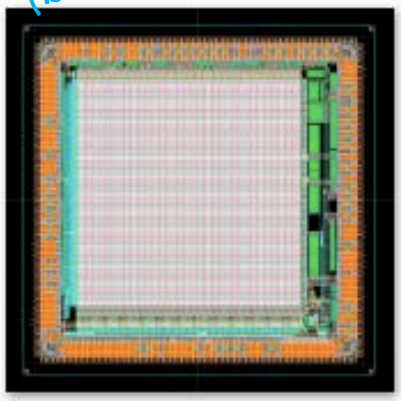
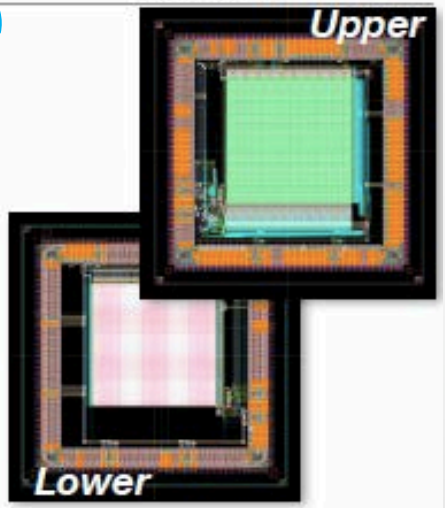
SOFIST PIXEL ARCHITECTURE

Start Vramp per beam train
Signals exceeding Vth
shift-register chooses* memory cell to record
⇨ analog signal recorded
timestamp voltage recorded

Recorded memories are digitized by column ADCs
(8bit has been implemented)
Zero-suppression applicable



SOFIST – IN DEVELOPMENT

	MX1850	MX2040	MX2166	
SOFIST	ver.1	ver.2	ver.3	ver.4 (3D)
	FNAL Beamtested (only analog)	FNAL Beamtested (both but in separate pixels)	Under evaluation (both in same pixel)	
				
Chip Size (mm^2)	2.9 x 2.9	4.45 x 4.45	6 x 6	4.45 x 4.45
Pixel Size (μm^2)	20 x 20	25 x 25	30 x 30	20 x 20
Pixel Array	50 x 50	64 x 64 (Time Stamp) 16 x 64 (Analog Signal)	128 x 128	104 x 104
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n* -type (Single SOI)	Cz *p* -type (Double SOI)	FZ *p* -type (Double SOI)	FZ *p* -type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Under evaluation	Delivered (Jan. 2017)		

delivered — Under 3D

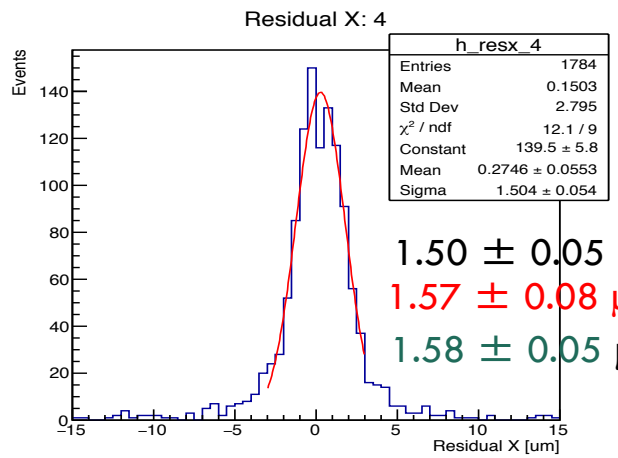
SOFIST-1 SPATIAL RESOLUTION

SOFIST residual to FPIX track (σ_track~0.57/0.65μm)
Bias=130V (~500um depletion) =>15V (~200μm depletion)
Readout: external 12-b ADCs =>on-chip 8-b ADCs

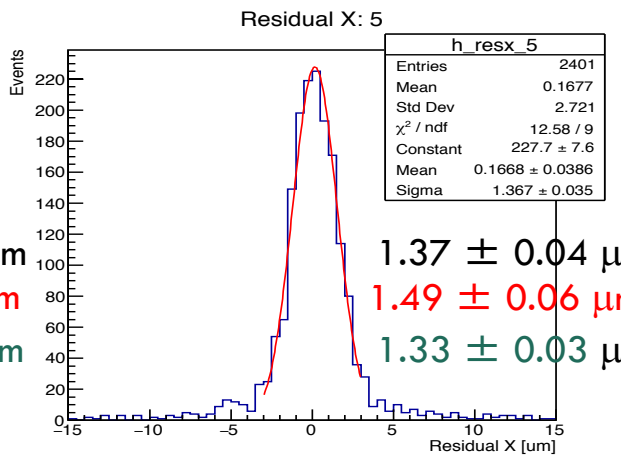
SOFIST#1(BPW14x14) SOFIST#2(BPW16x16)

plots for "black case"

Residual X

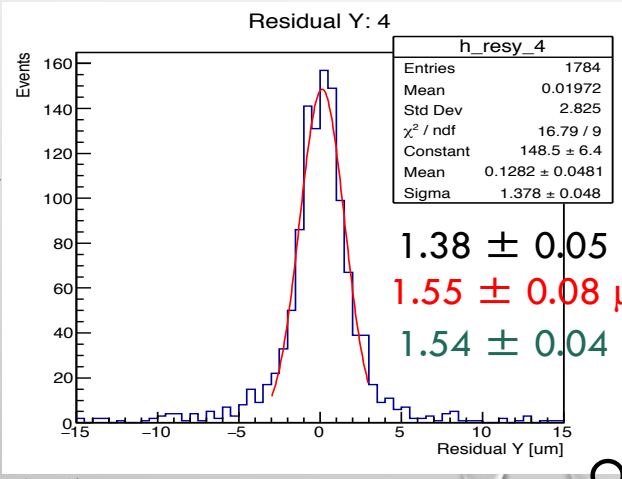


1.50 ± 0.05 μm
1.57 ± 0.08 μm
1.58 ± 0.05 μm

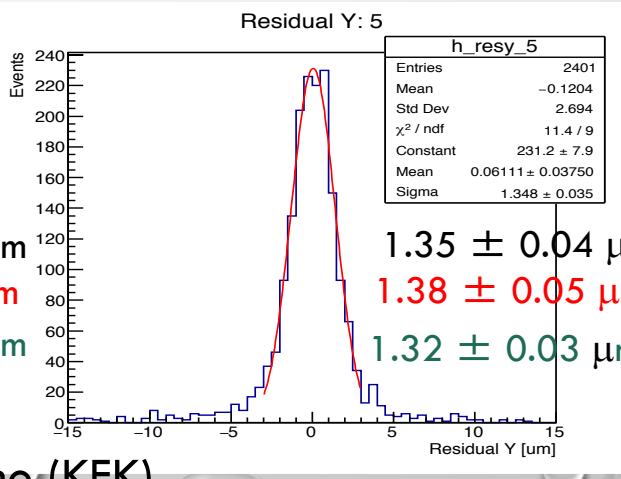


1.37 ± 0.04 μm
1.49 ± 0.06 μm
1.33 ± 0.03 μm

Residual Y



1.38 ± 0.05 μm
1.55 ± 0.08 μm
1.54 ± 0.04 μm

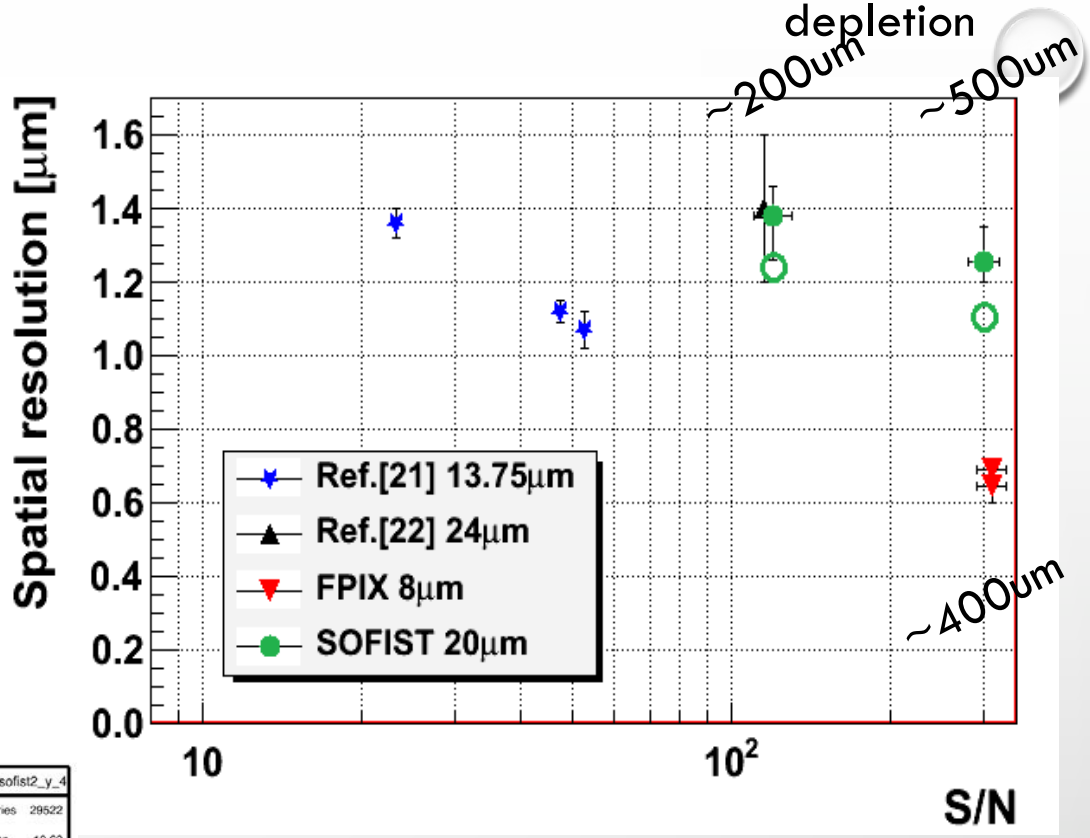


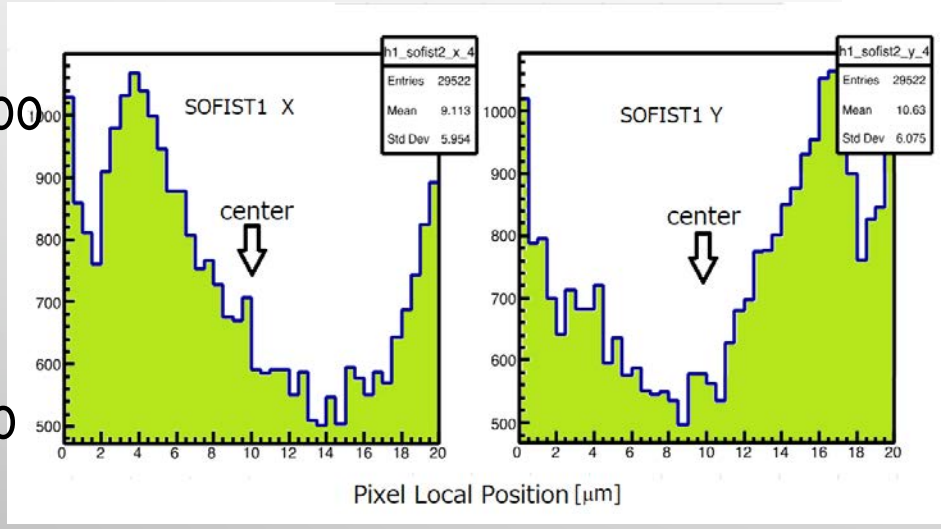
1.35 ± 0.04 μm
1.38 ± 0.05 μm
1.32 ± 0.03 μm

S/N~300 (130V)
~120 (15V)

SOFIST-1 SPATIAL RESOLUTION

- Track uncertainty (0.6um) subtracted
  Compatible with DEFFET ([22])
- η correction may improve further

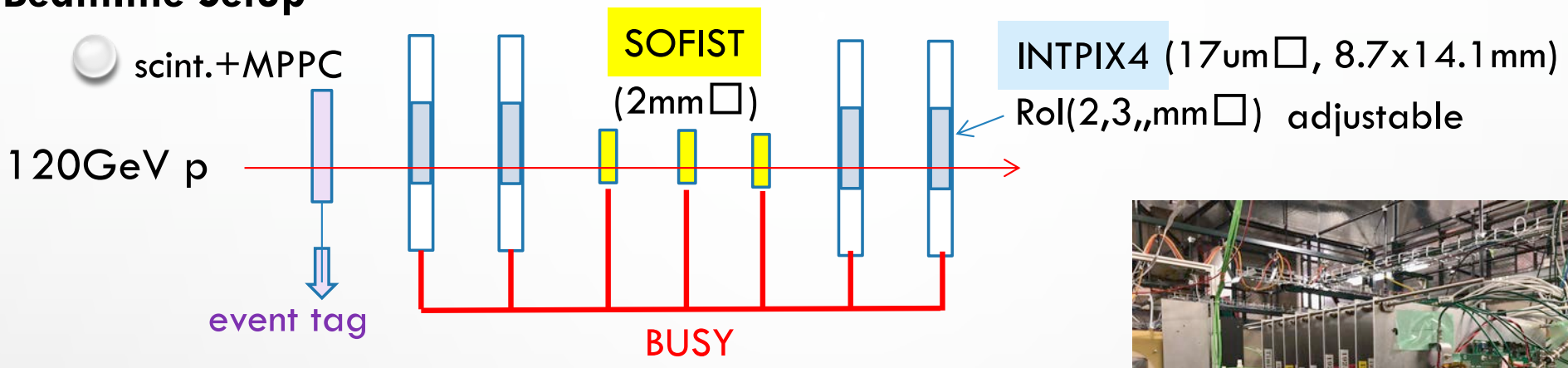


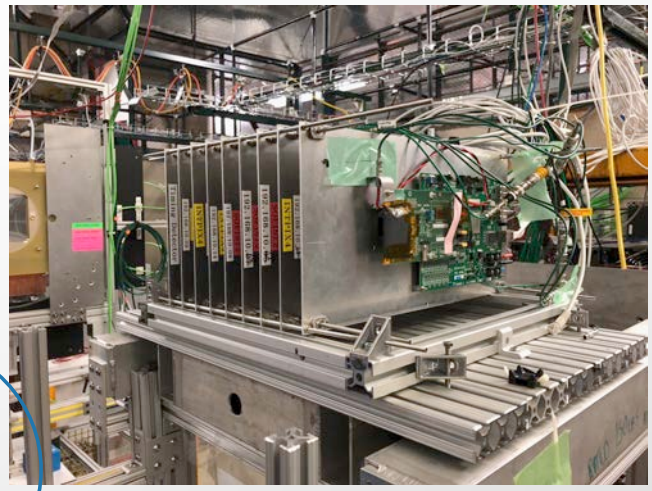


Ono (KEK)

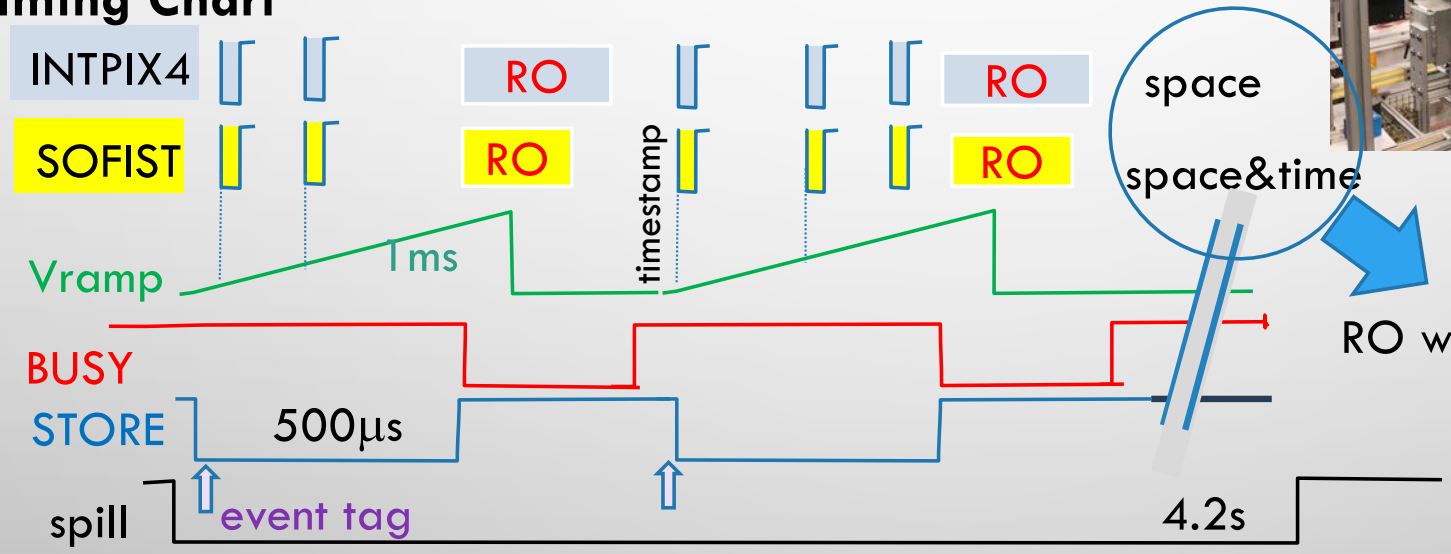
SOFIST-2 BEAM TEST 2018MAR

Beamline Setup





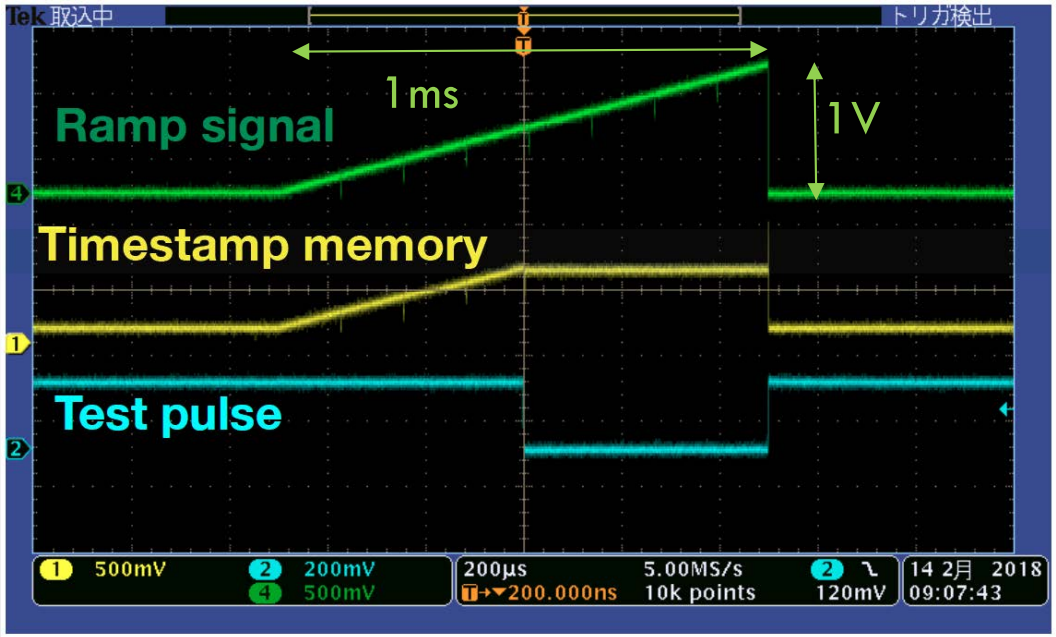
Timing Chart

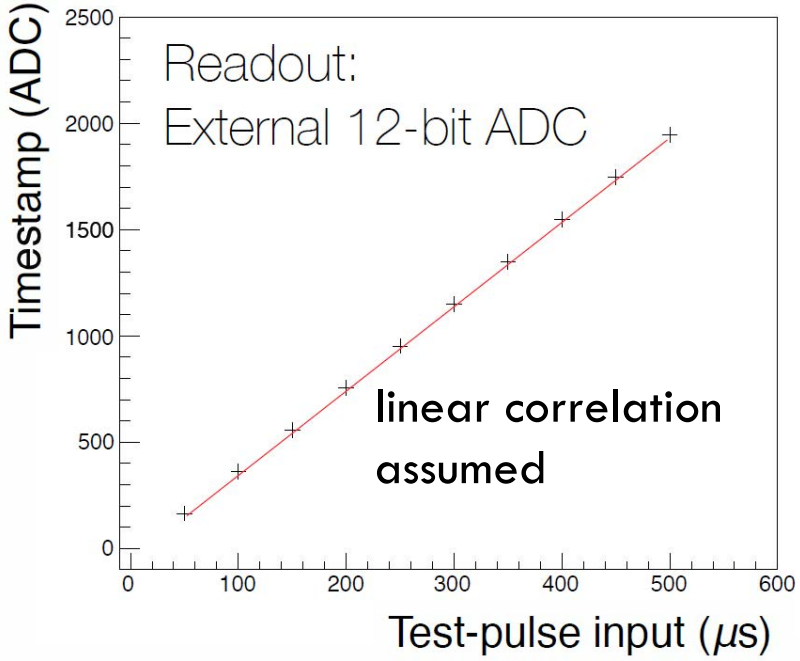


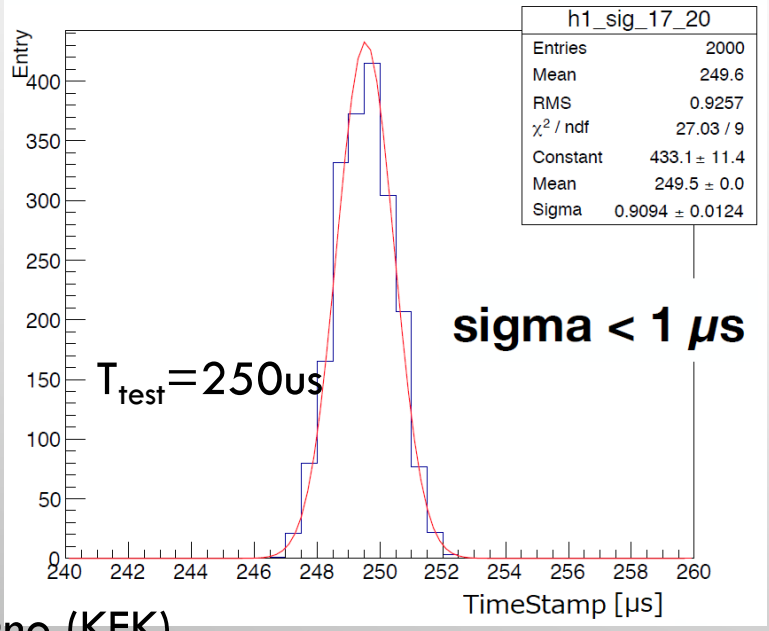
RO with external 12-bit ADCs

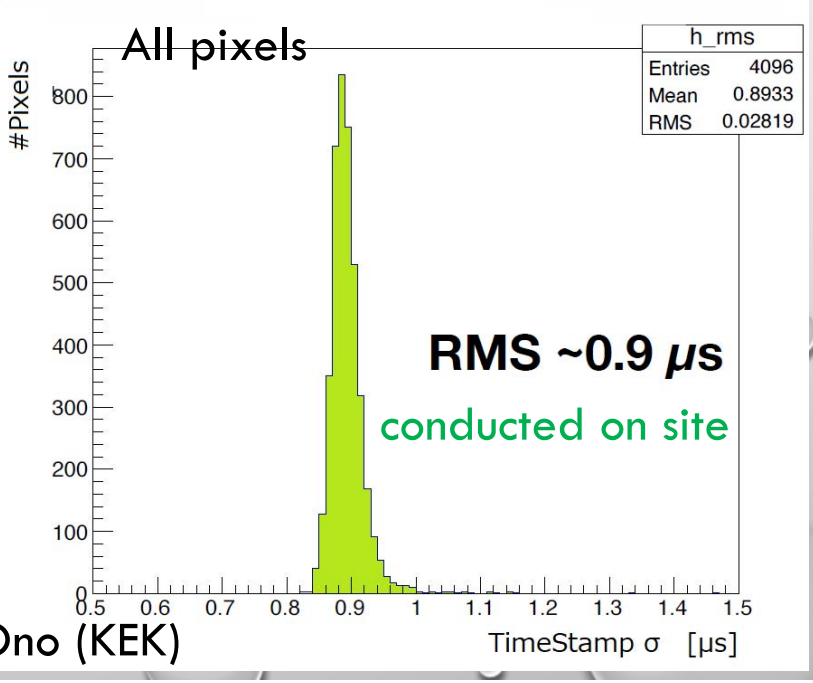
SOFIST-2 TIMESTAMP CALIBRATION

conducted on site



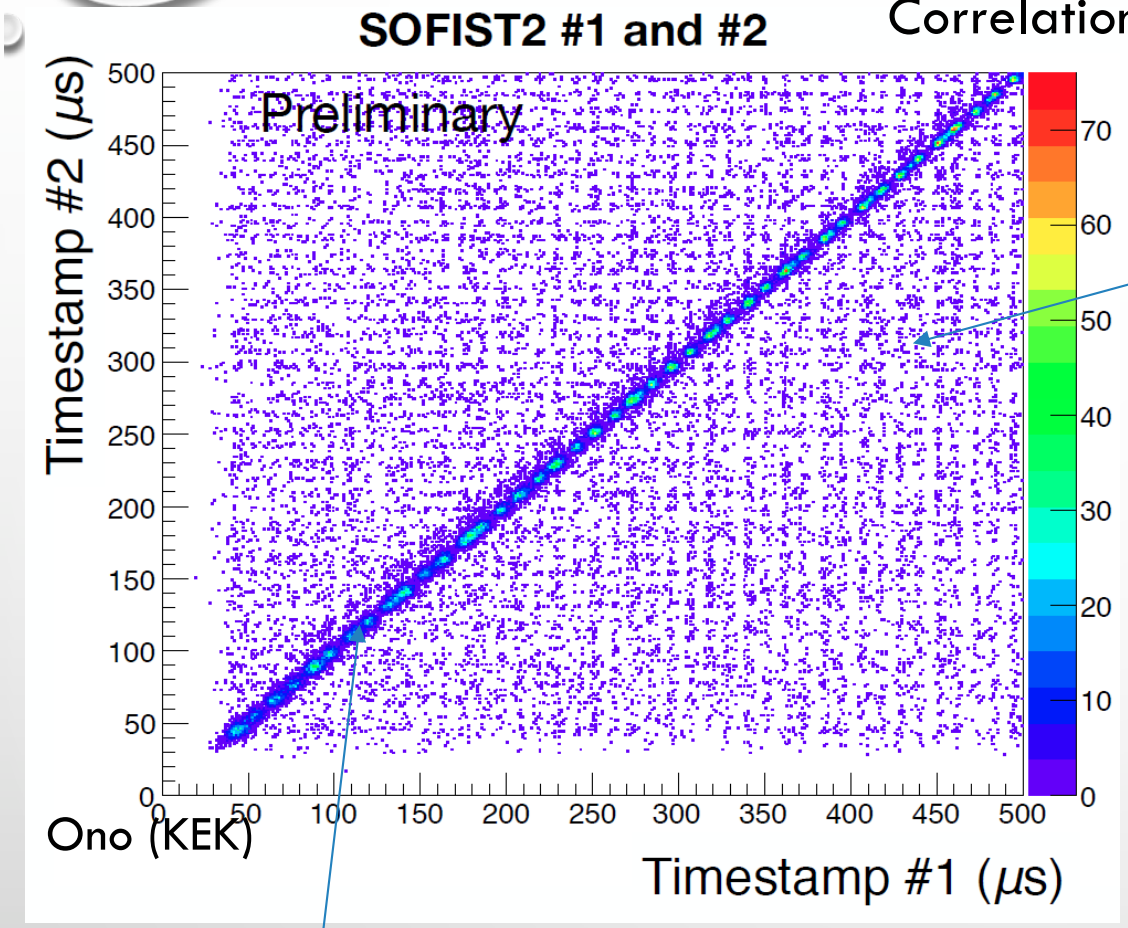




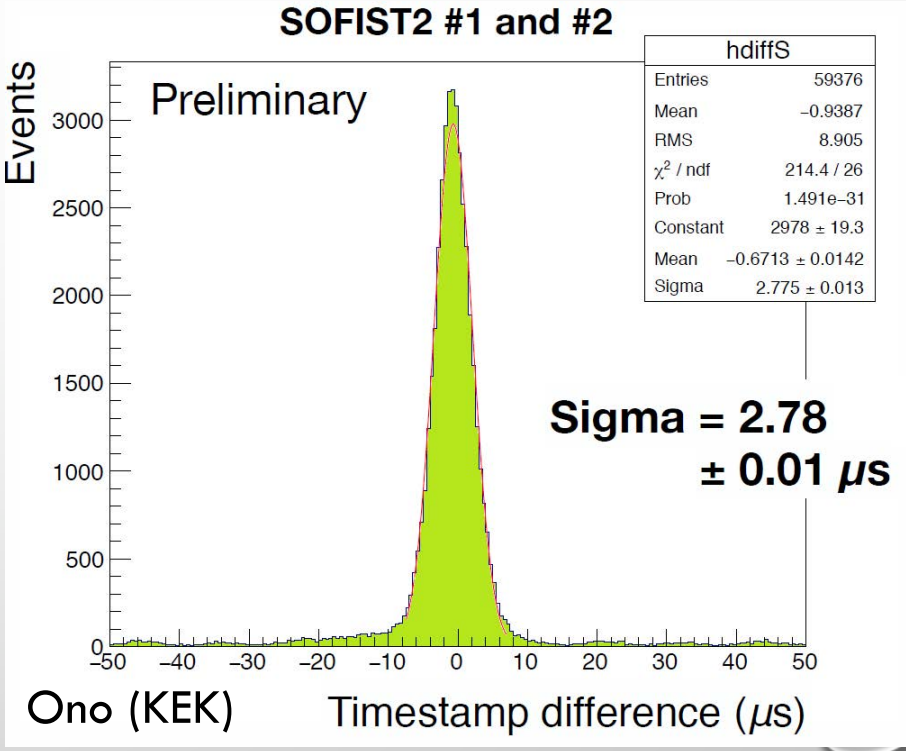


SOFIST-2 TIMESTAMP CORRELATION

Correlation of timestamps in two SOFISTs



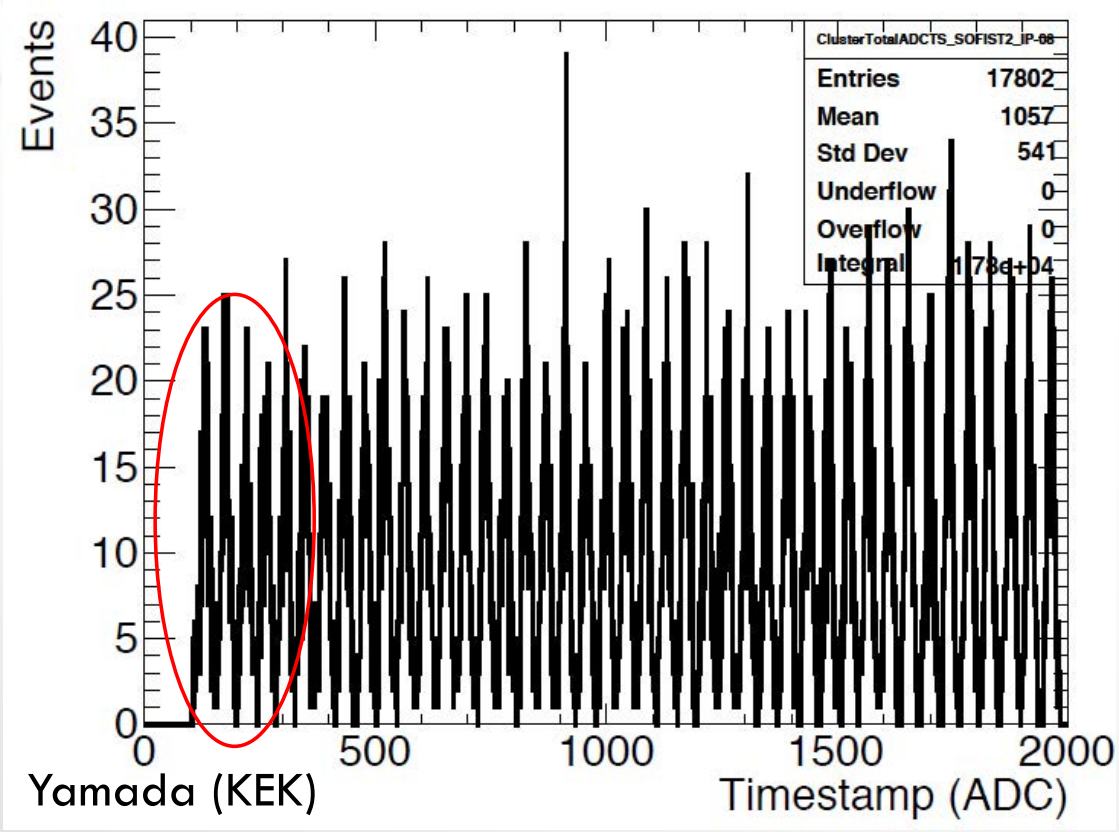
Overlapping events in same 500us gate

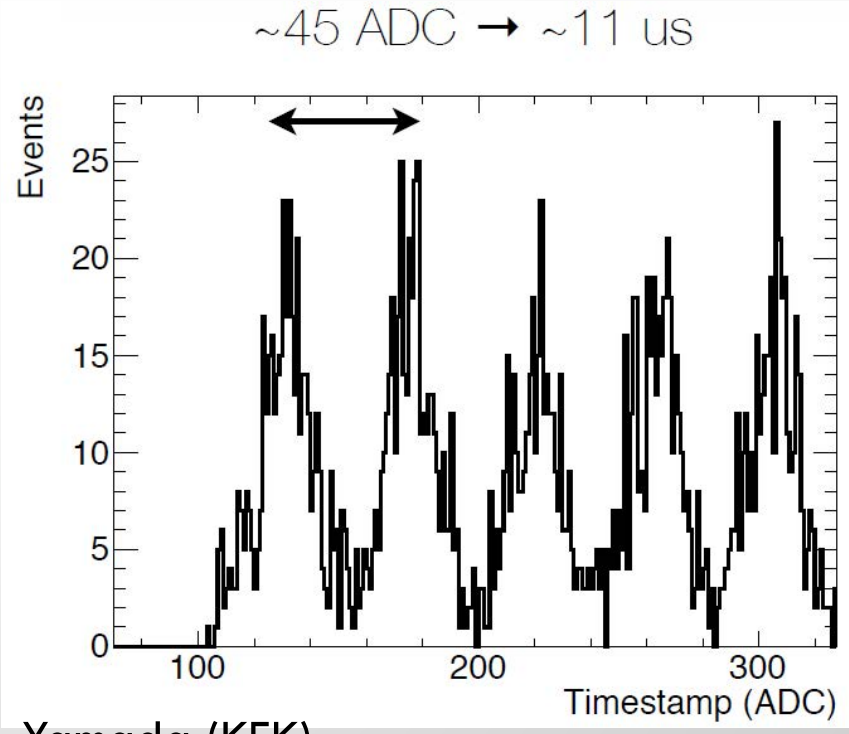


Periodic clusters?

Timestamp resolution
2.78/√2=1.89us

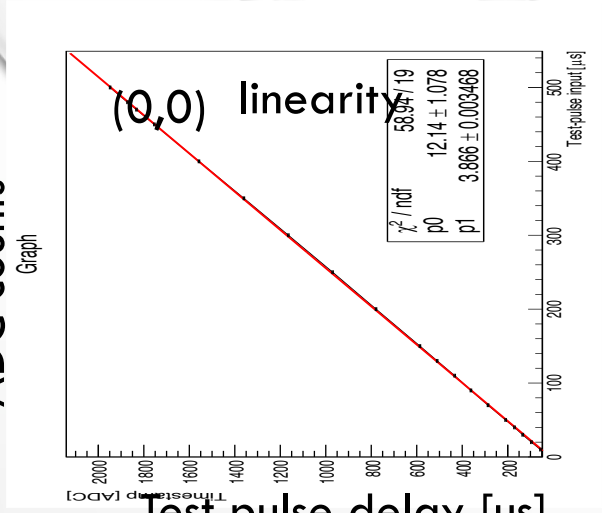
SIZE OF FNAL MAIN INJECTOR (MI)





Beam structure due to bunch rotation in the MI: 11us⟶3.3km (3319m actual)

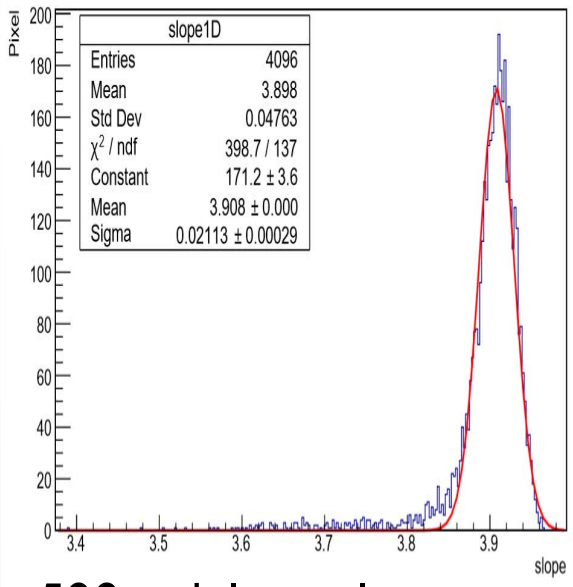
SOFIST-2 TIMESTAMP PRECISION

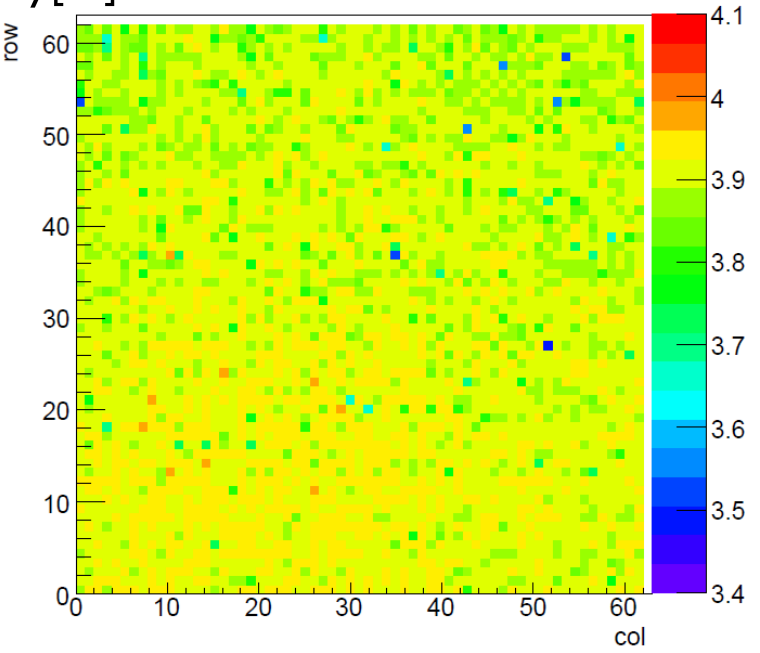


Murayama (Tsukuba)

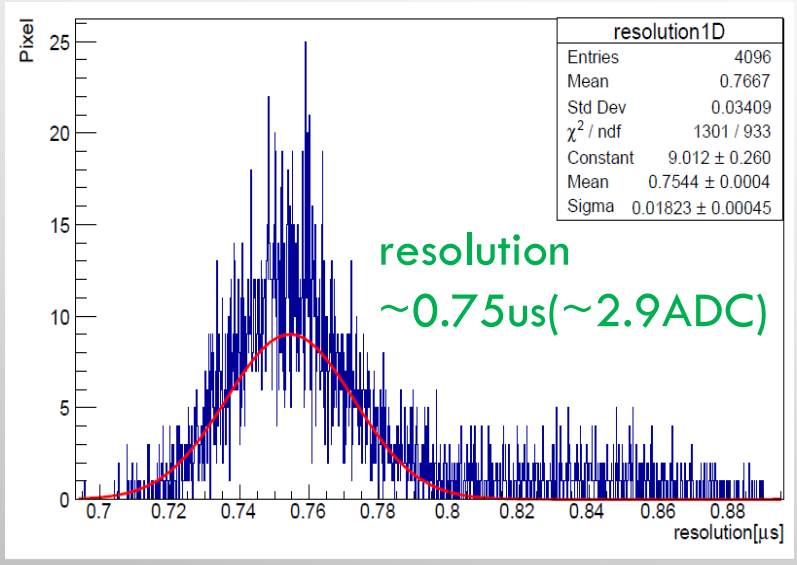
conducted on testbench

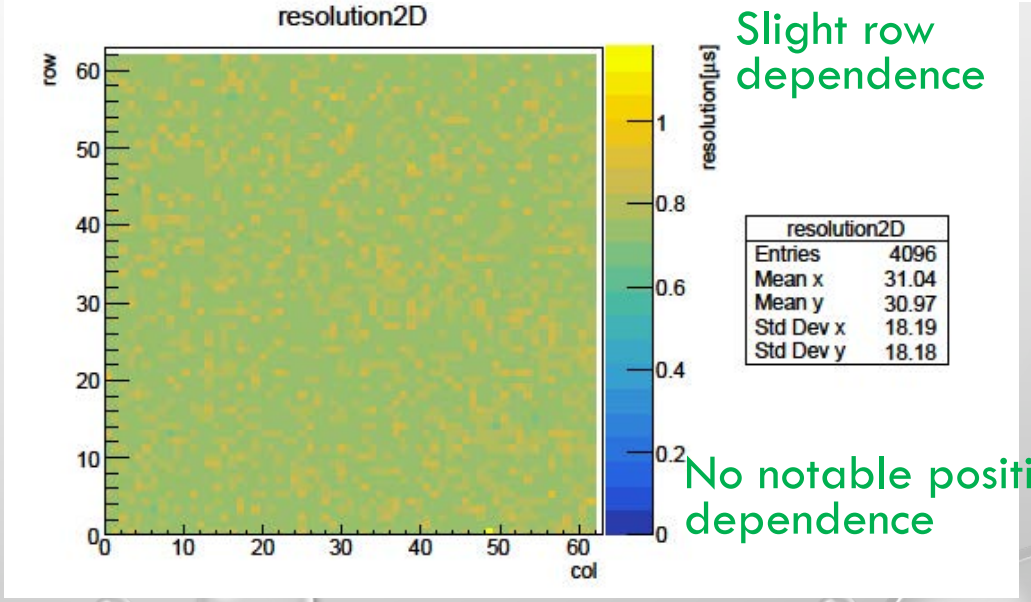
ΔADC/Δdelay[us]





Time spread for 500us delay pulses

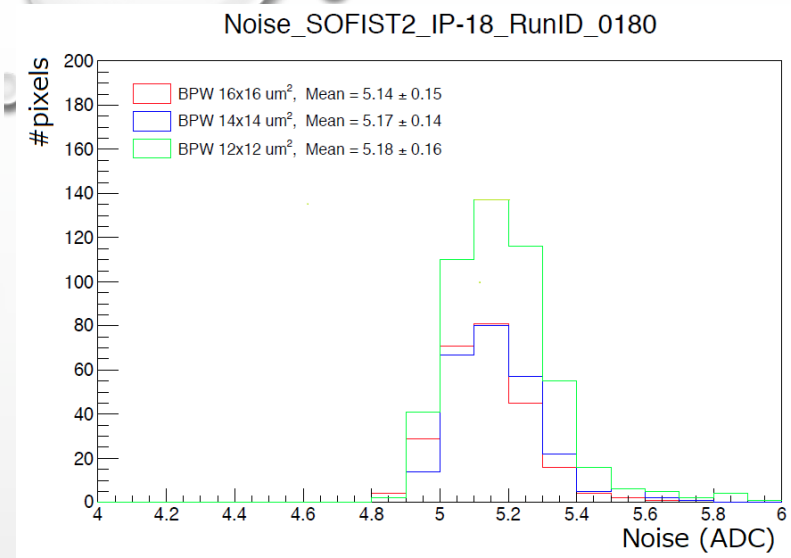


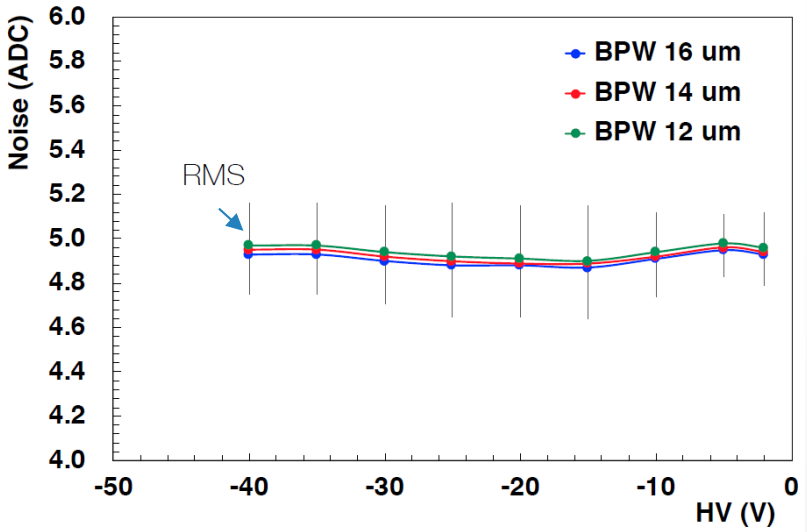


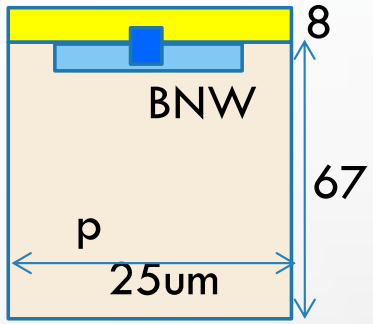
Slight row dependence

No notable position dependence

SOFIST-2 ANALOG SIGNAL

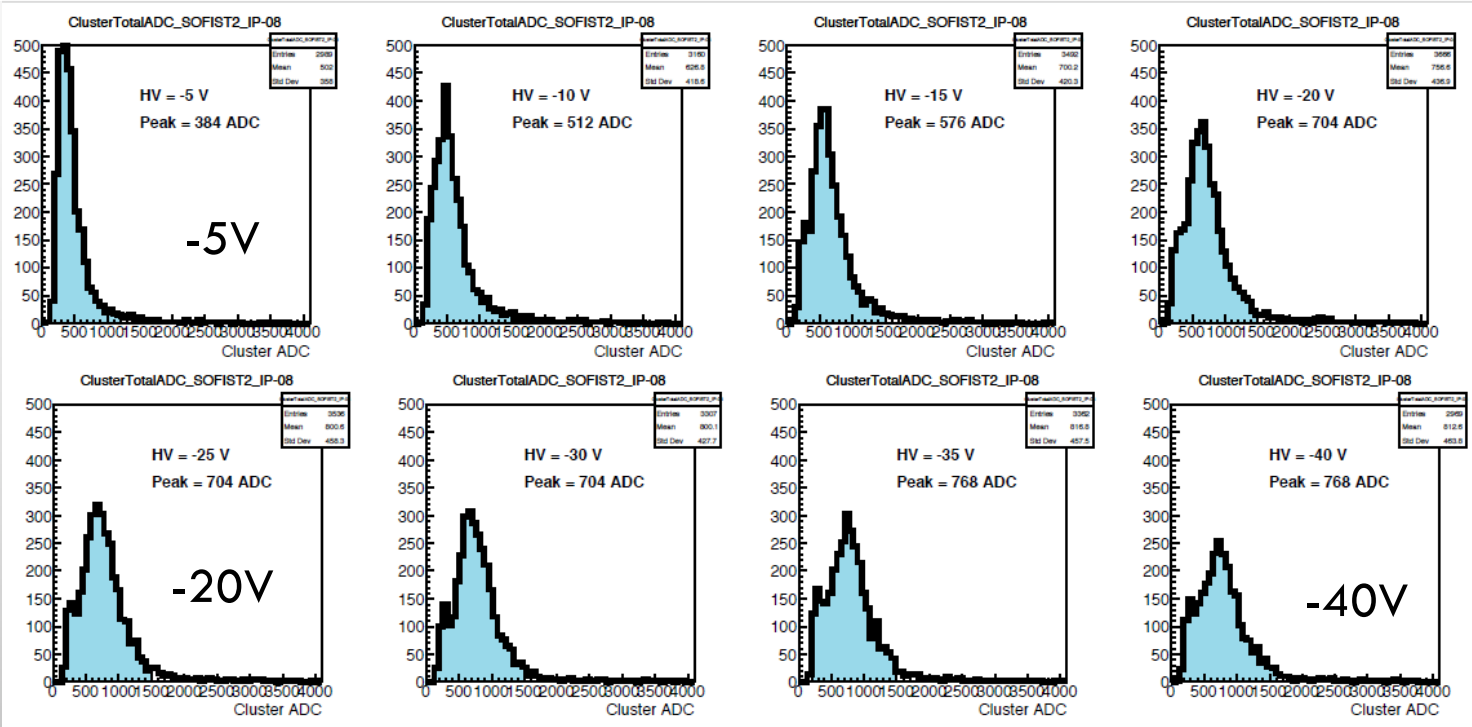




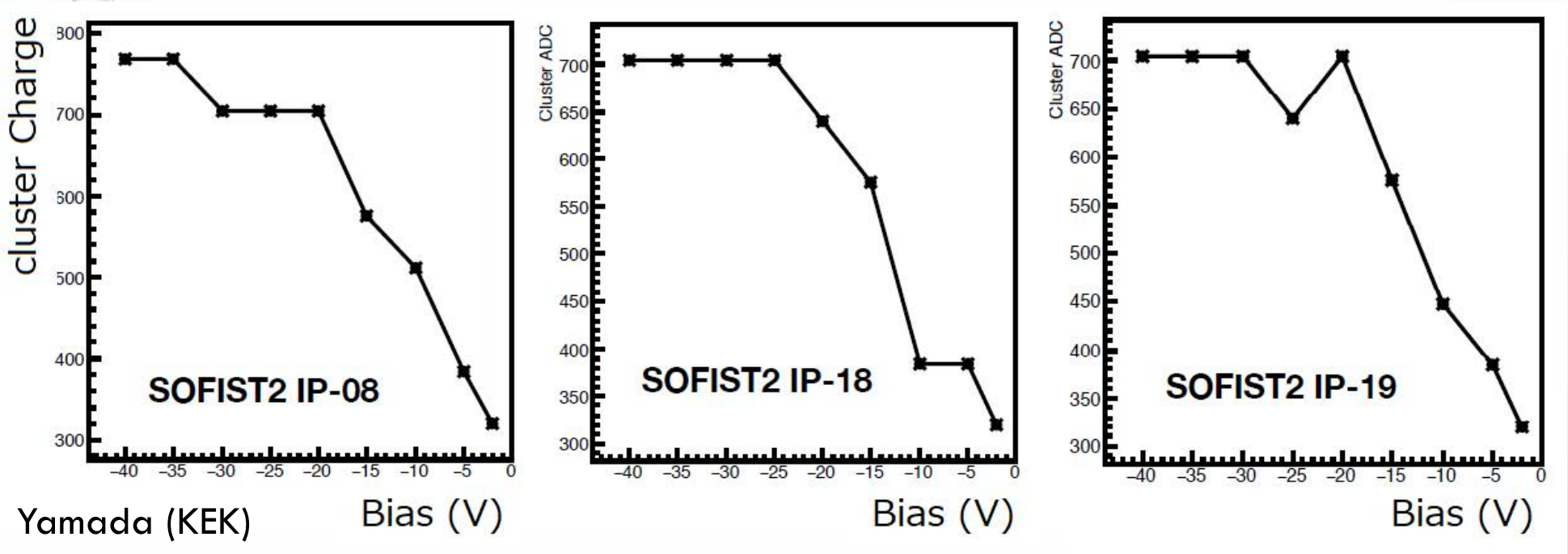


Yamada (KEK)

Cluster charge
(HV dependence)



SOFIST-2 FULL DEPLETION



Yamada (KEK)

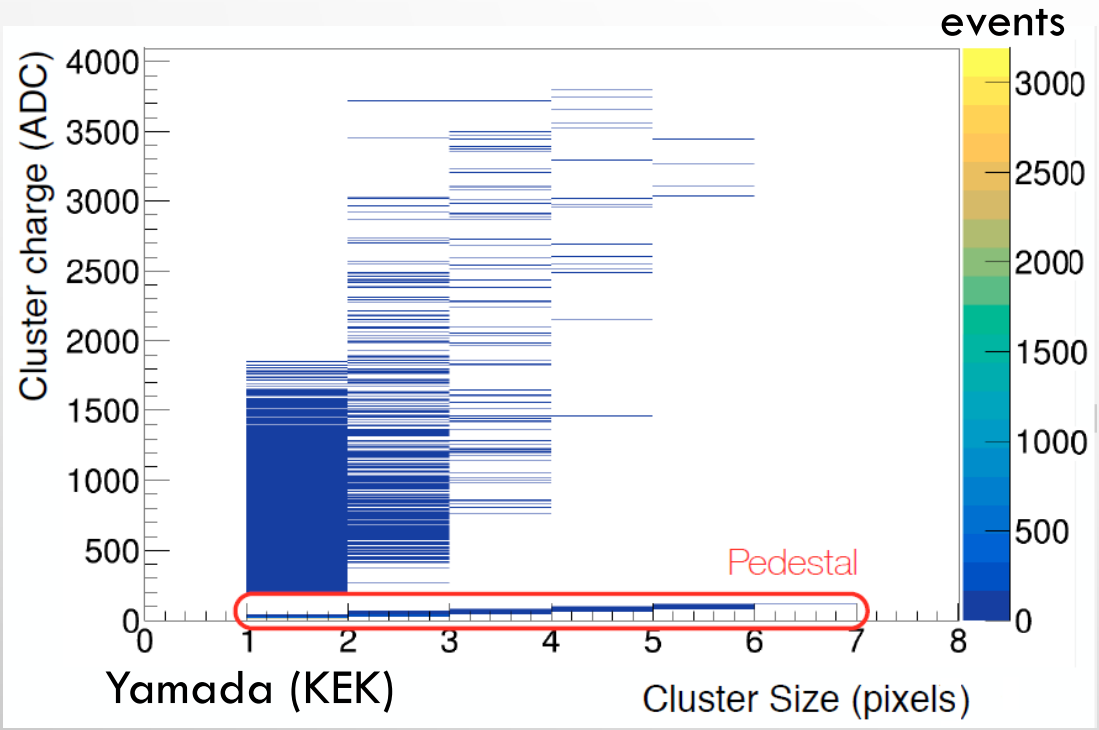
Full depletion expected ~30V for $9 \times 10^{12}/cm^3$ (0.5kΩcm) concentration (measured)

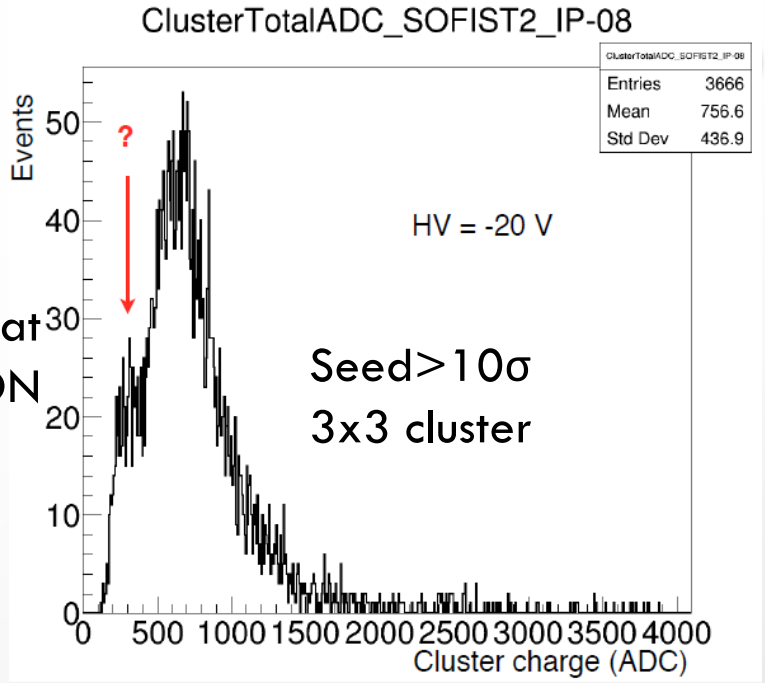
S>700 ADC (N~5 ADC) for 67um thickness

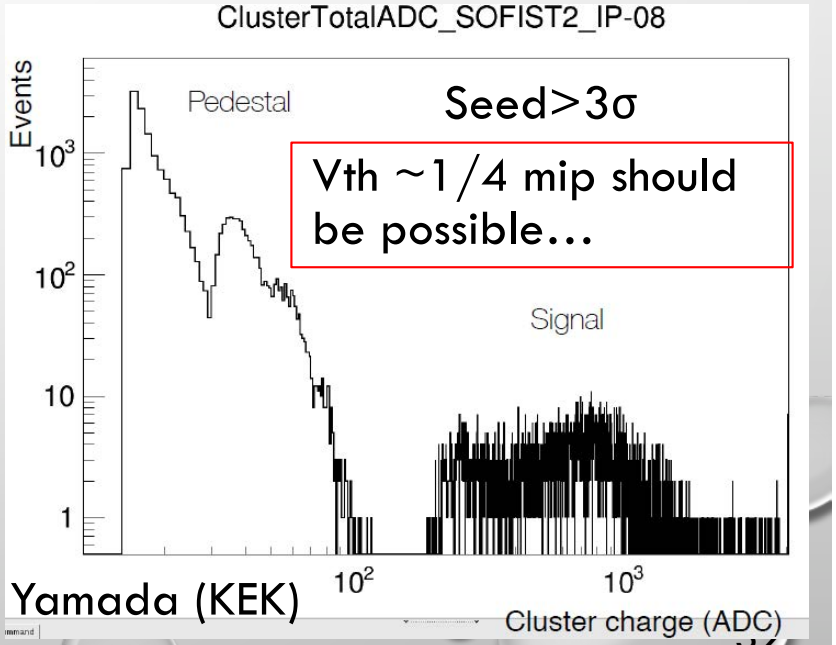
SOFIST-2 CLUSTER CHARGE

Mostly one-cluster events
Vth ~1/2 mip

peak~300ADC: X-talk at Comparator ON

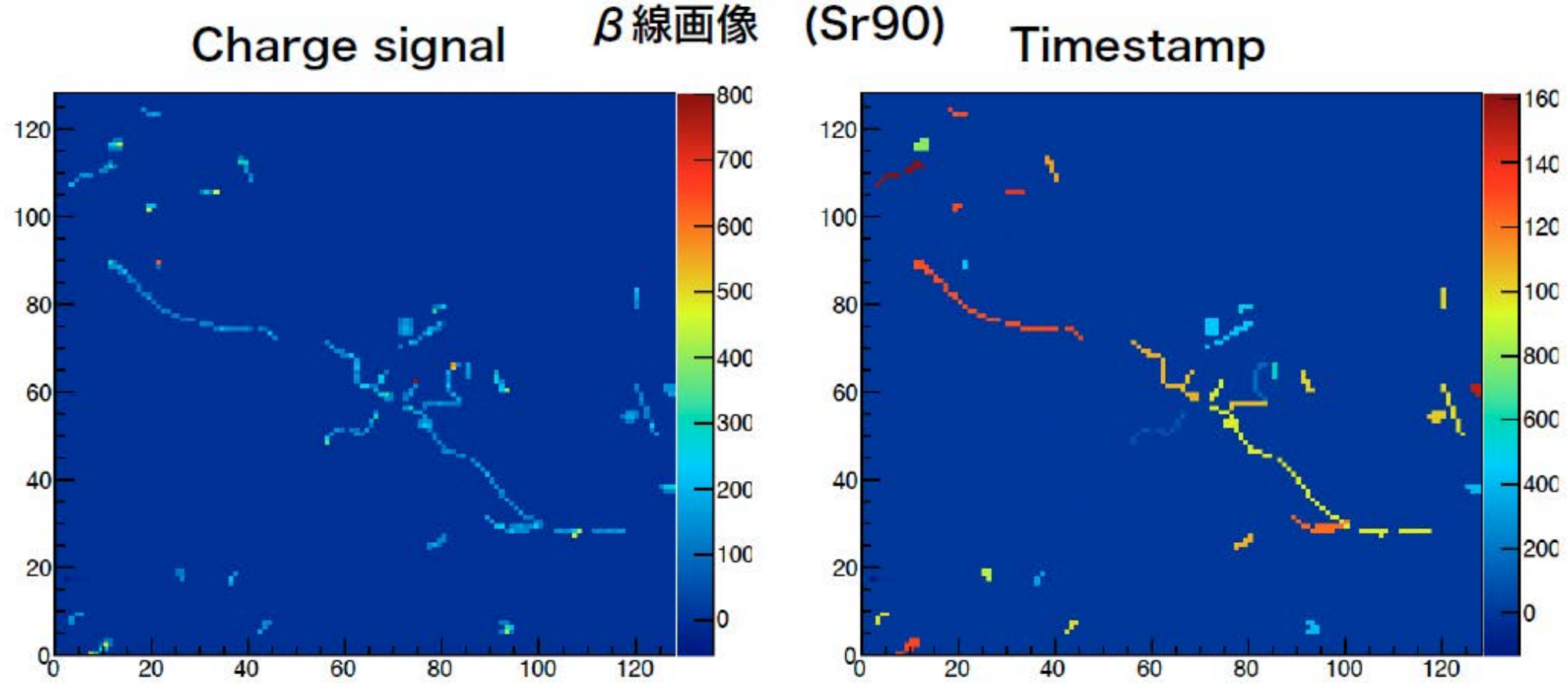




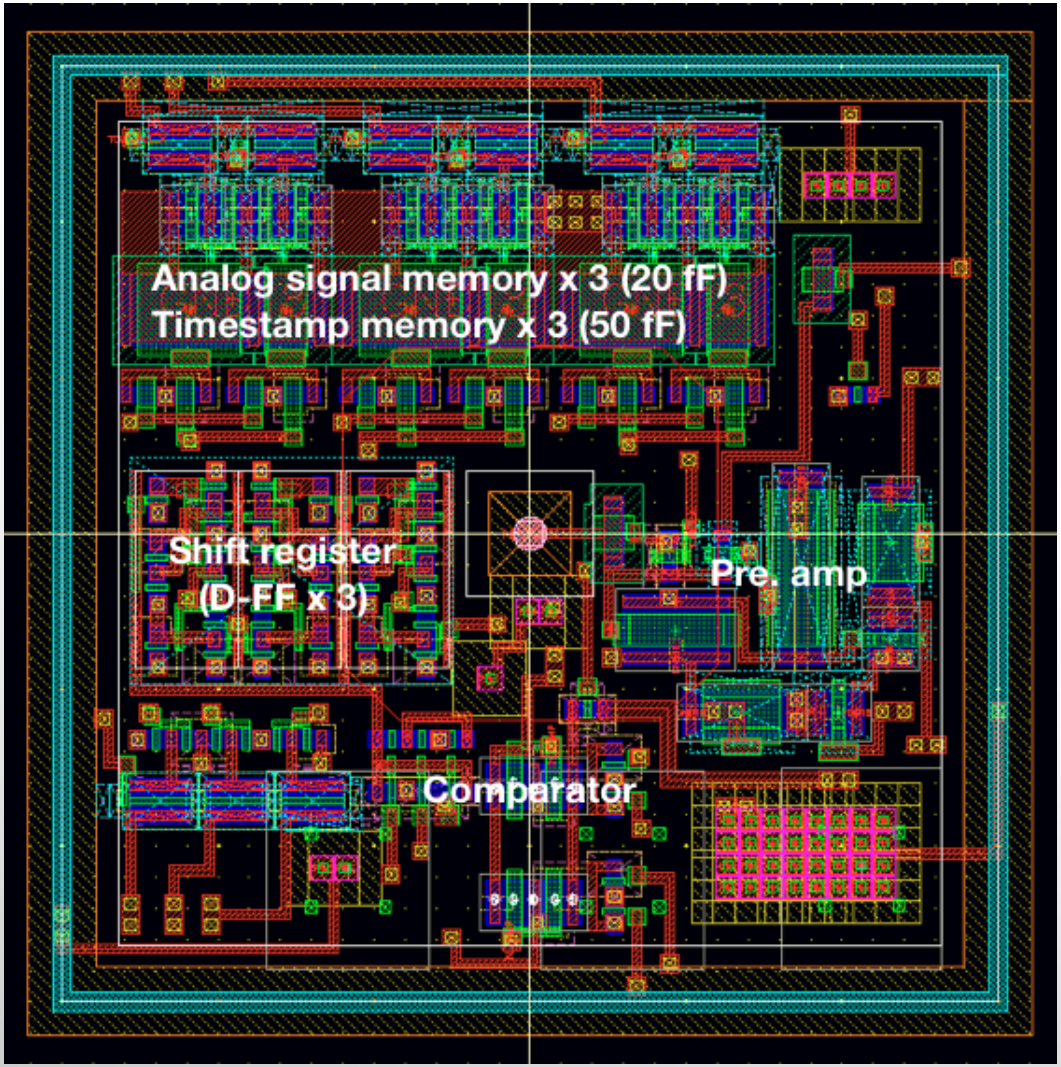


SOFIST-3 – QUICK TEST

Both functions implemented on 30um pixels

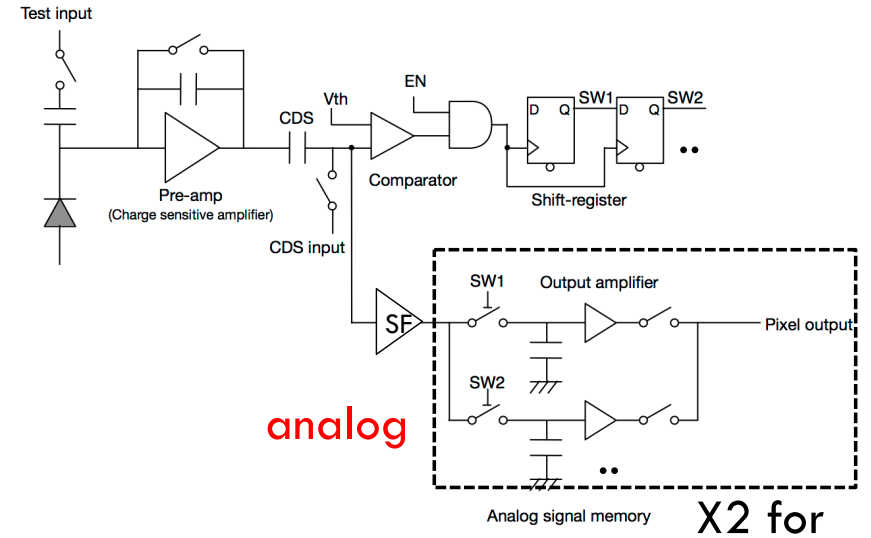


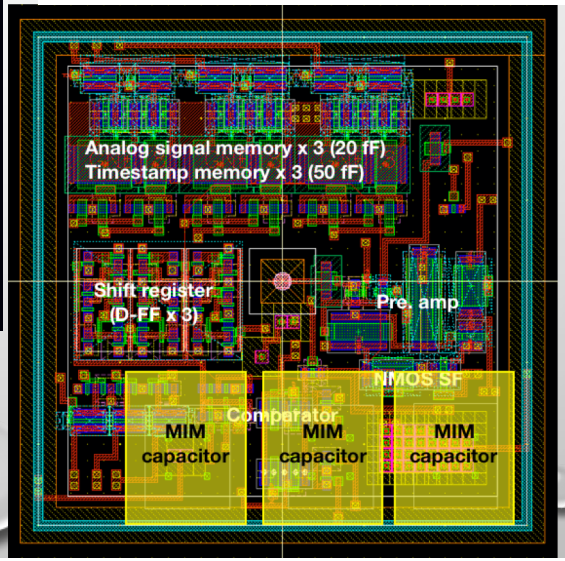
SOFIST-3 – PIXEL LAYOUT



30um

Yamada (KEK)



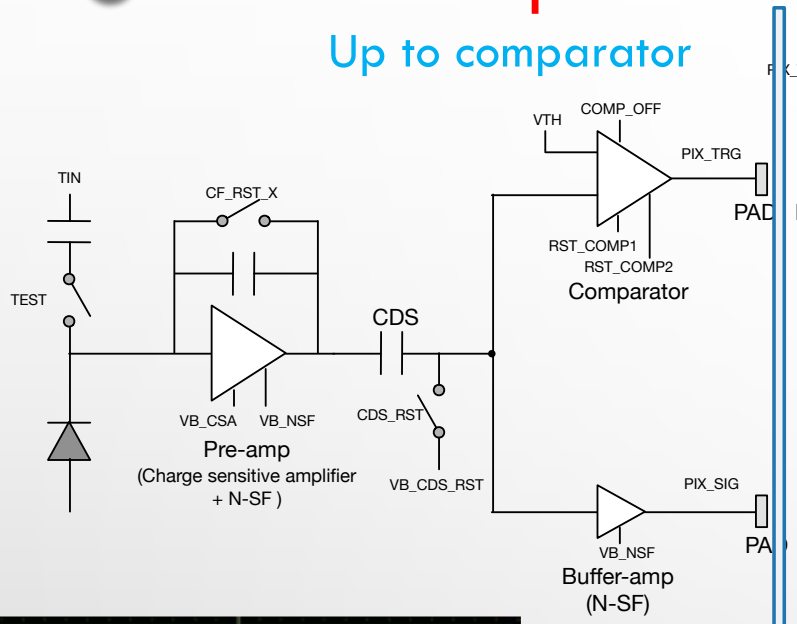


MIM(50fF, 1.5fF/um^2)
1 for CDS
2 for comparator

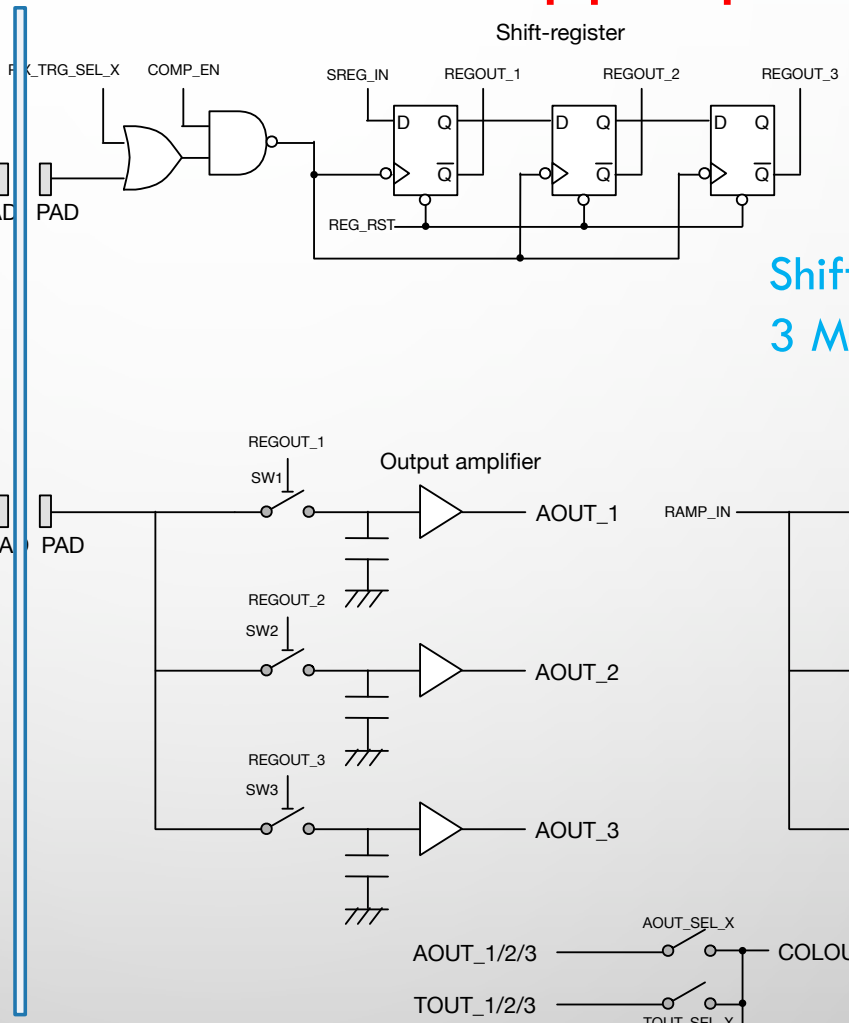
SOFIST VER.4

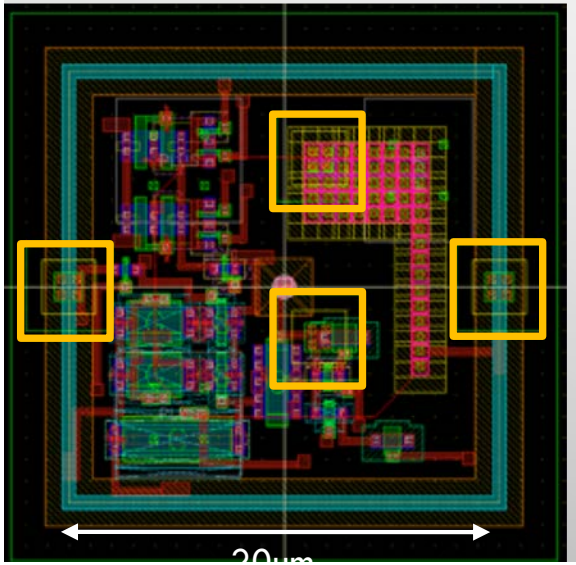
Lower pixel

Up to comparator



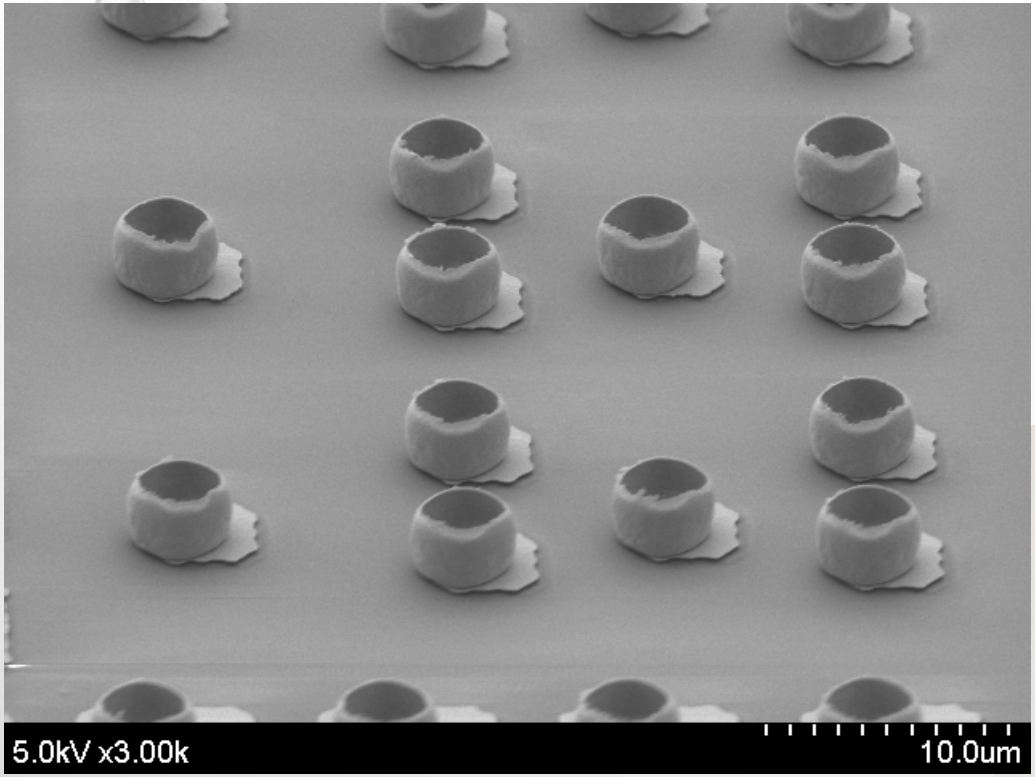
Upper pixel

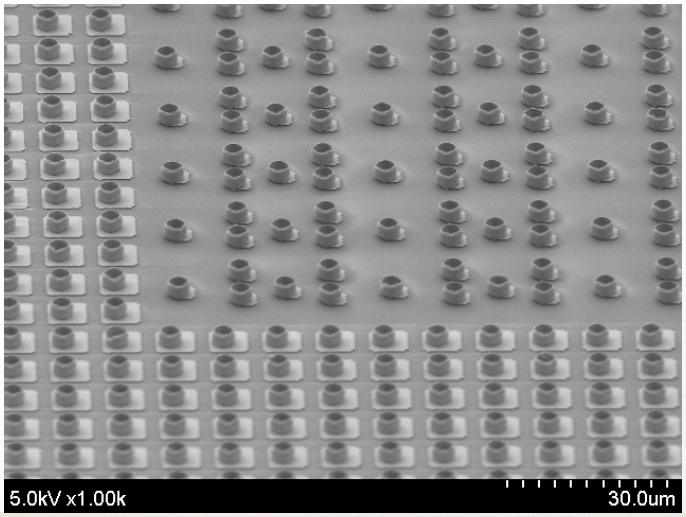




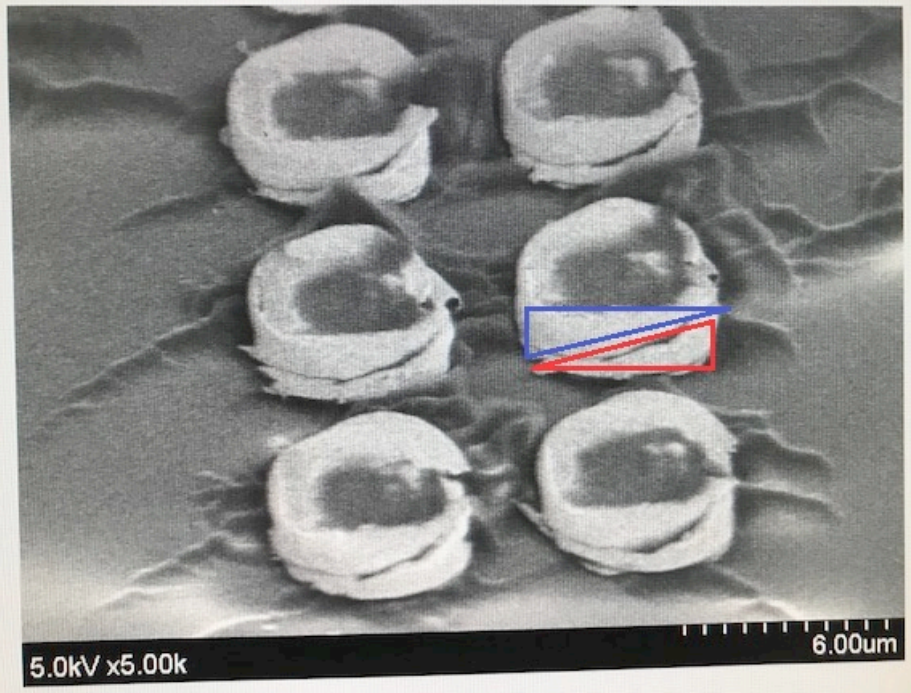
3D IS COMING (SOFIST-4)

Cylinder-type is more reliable





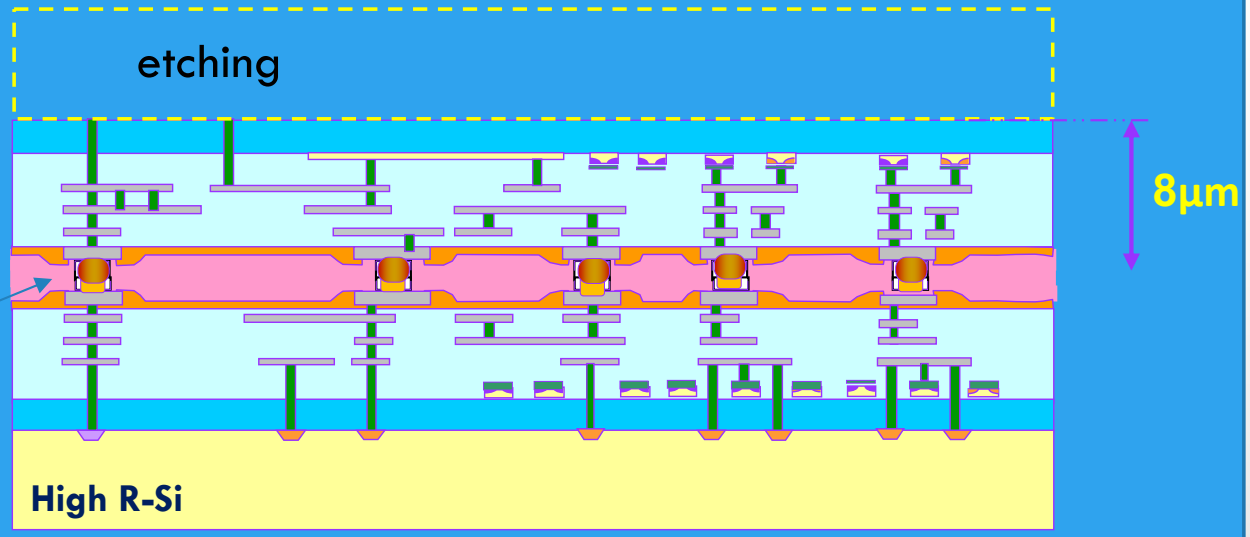
T-Micro　slight mis-alignment to UBM ⇒corrected



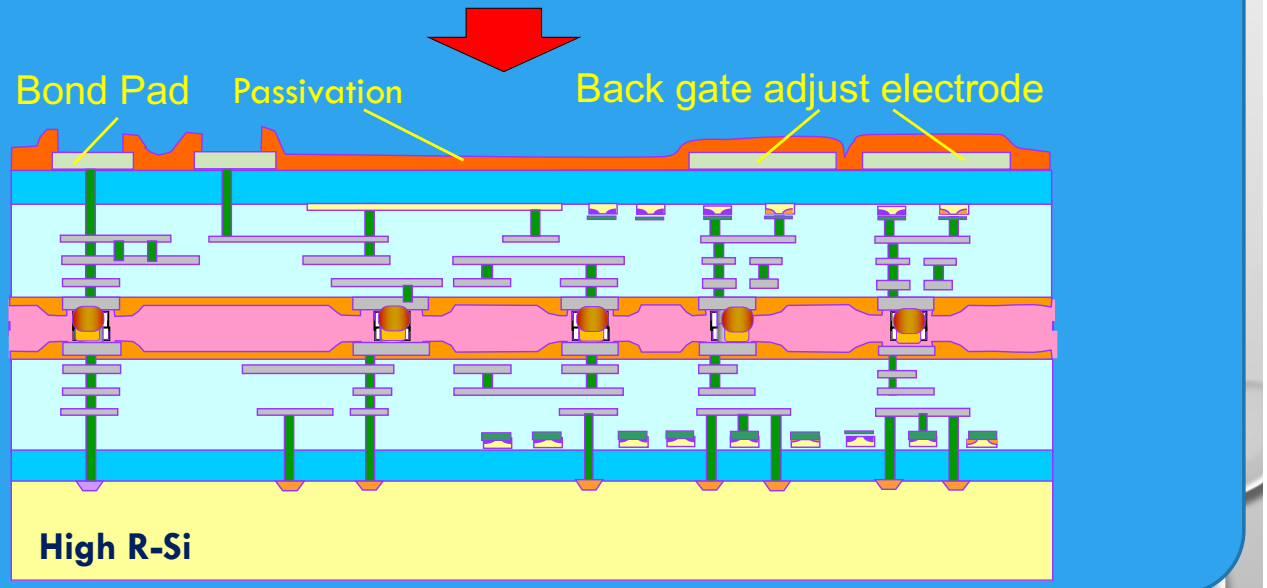
Upper&lower bumps are stacked well
(peel off one sensor layer)
Bonding<200degC

REMAINING PROCESSES (SOFIST-4)

(d) Bulk-Si removal

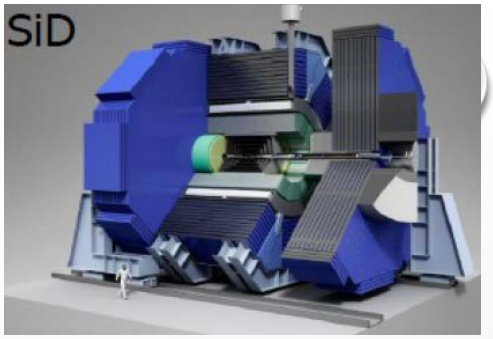


(e) Pad patterning and passivation



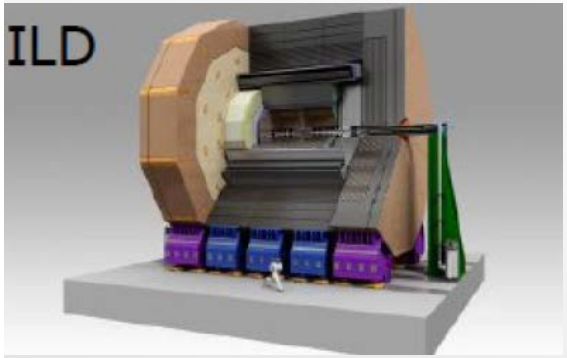
T-Micro

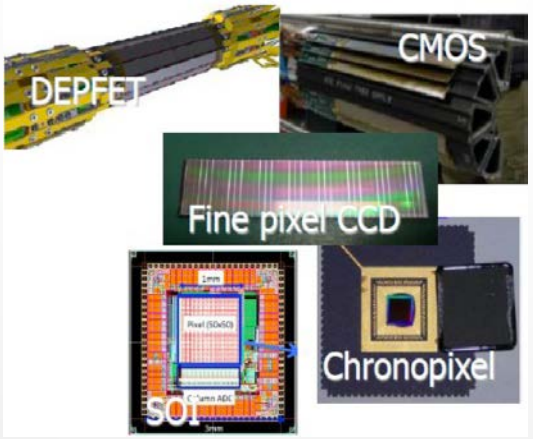
ILC 1-PAGE SUMMARY

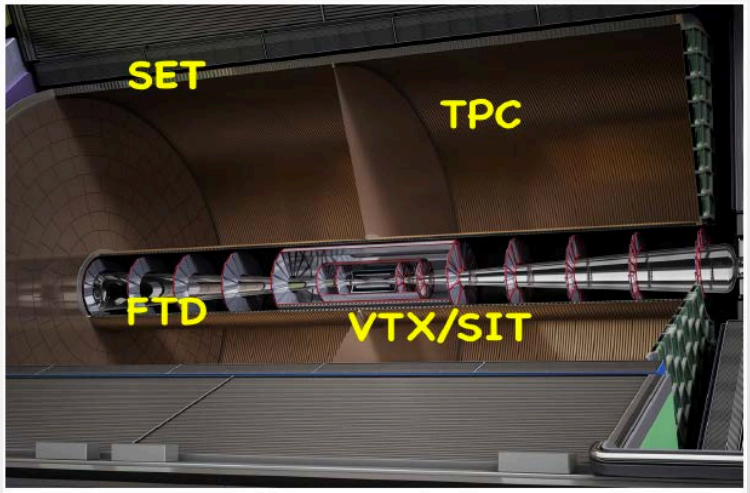


SID: VTX AND SILICON TRACKER

- Baseline pixel pitch: 20×20 μm^2
- Technology options: either monolithic CMOS chip ➡ Chronopix or 3D vertically integrated silicon







ILD: VTX & Silicon Tracking System

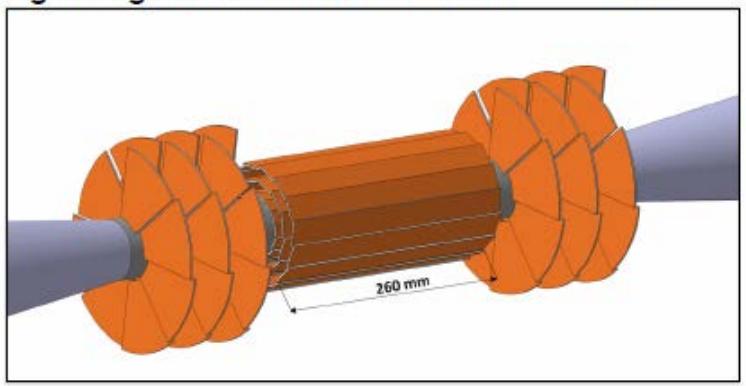
- Barrel (VTX): 3 double-sided ladders
  - Inner layers (< 300 cm^2), SIT: priority on readout, speed and σ_{sp}

    16×16/80 μm^2 pixels and binary o/p: t_{ro} ~ 50/8 μs and σ_{sp} ~ 3/5 μm
  - Outer layers (~3000 cm^2), SET: importance of power consumption and σ_{sp}

    35×35 μm^2 pixels and 3-4 bit charge encoding: t_{ro} ~ 100 μs and σ_{sp} ~ 4 μm
  - R&D on several technologies, namely DEPFET, FPCCD, SOI and CMOS

CLIC 1-PAGE SUMMARY

Lightweight silicon vertex detector:



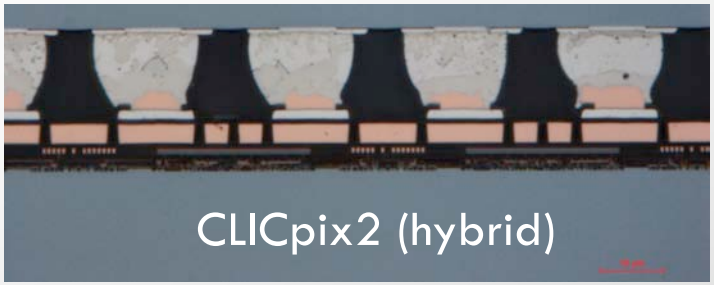
To reach impact parameter resolution:
- Spatial resolution: 3 µm
- Material: 0.2 % X0/layer

To reduce impact of beam-beam background:
- Pixel size of 25 µm x 25 µm, timing resolution O(ns)

Moderate radiation exposure (~104 below LHC):
- NIEL: < 10^{11} neq/cm2/y, TID: < 1 kGy / year

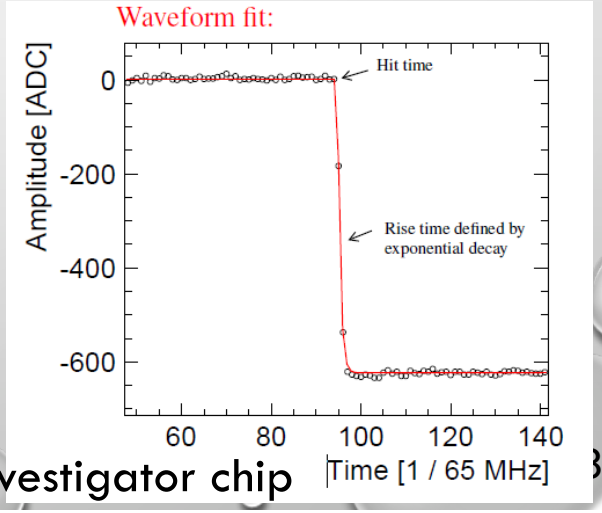
CLICpix: - 4 bit ToT and ToA, 64 x 64 pixels
CLICpix2: - 5 bit ToT and 8 bit ToA,128 x 128 pixels
- 65 nm CMOS technology
- Pixel size of 25 µm x 25 µm
- Power pulsing

Bump bond or
Capacitive coupling



Cracow SOI test-chip produced in 200 nm LAPIS SOI process
- pixel size >= 30 µm x 30 µm σ=3um
- High resistivity substrate with thickness of 500 µm

HR-CMOS
Spatial resolution below 7 µm for threshold values of ~400e-
- Fully efficient operations to threshold values below ~400e-
- Timing resolution ~ 6 ns



In Investigator chip

SUMMARY (SOI)

- 5-year Grant-in-Aid (2013-2017) accelerated development/application of various SOI devices.

- SOFIST has been tested in FNAL beam
  - SOFISTv1 <20um pixel size>
    - spatial resolution:
    - 1.3 um(500um)-1.4 um (200um) with no η-correction applied
  - SOFISTv2 <25um pixel size>
    - time resolution: 1.89us (linear calibration)
    - good S/N~120 for 67um thickness
    - cluster size~1 (Vth was set slightly high)
    - - spatial resolution results to come shortly

- SOFISTv3 is to be beam tested
- SOFISTv4 fabrication is underway
- Submitting new 5-year Grant-in-Aid application