SOFIST, an SOI based pixel sensor for the ILC

SOFIST: SOI Fine measurement of Space and Time

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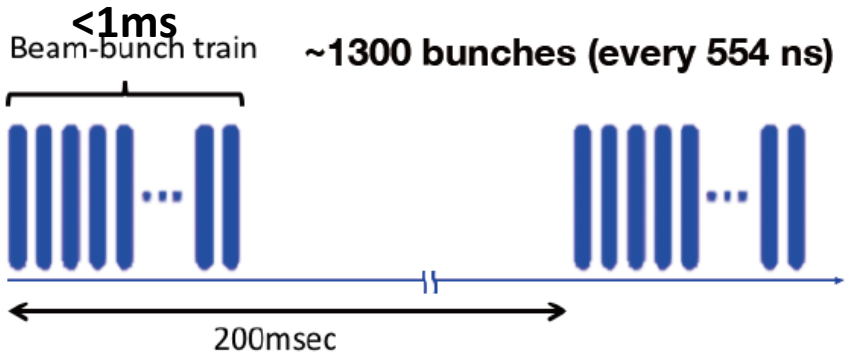
and the SOIPIX collaboration

*now at SONY Co.Ltd

Vertexing at the ILC

- Spatial resolution near the IP better than 3 μm
- Material budget below 0.15% X_0/layer
- Low-power ASICs (~50mW/cm^2)+gas-flow cooling
- The first layer located at a radius of ≥ 1.6 cm
  - Pixel occupancy not exceeding a few %
  - Radiation: TID<1kGy/y, NIEL<10^{11} n/cm^2/y



- We choose SOI monolithic, pixel size 20x20 μm
  - store data during the train, readout them in between trains
  - 3 memories each for the signal charge and arrival time

⇒ SOFIST (SOI fine measurements of space and time)

Occupancy /(20μm)^2/train and the efficiencies (vs #memories) at the innermost layer

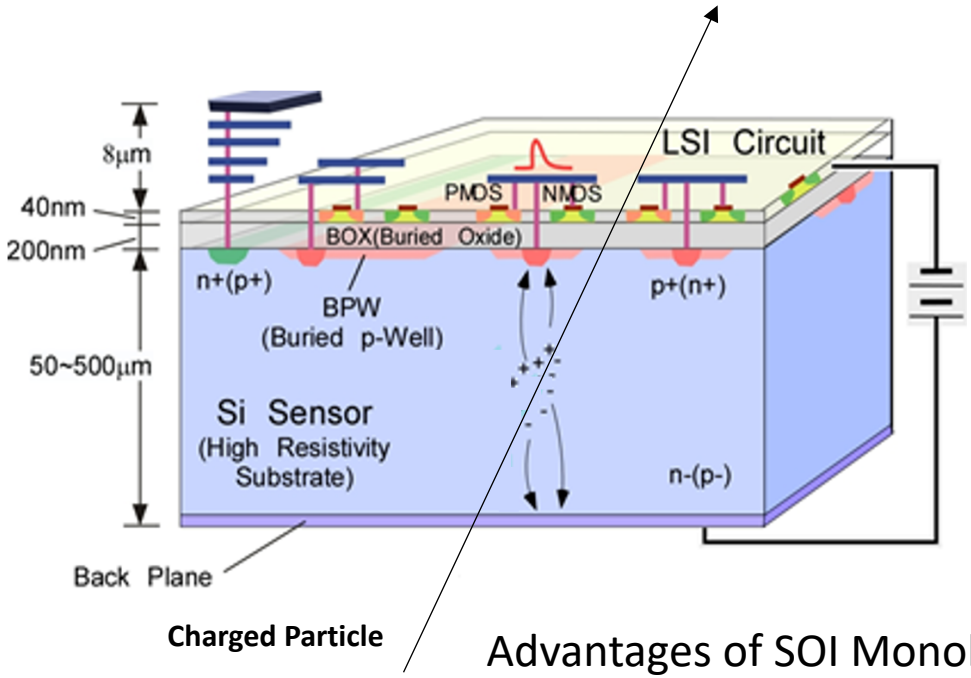
E_{CM}(GeV)	λ	Σ $e^{-\lambda}(\lambda)^N/N!$ (%)						
		N=0	1	2	3	4	7	8
250	0.09	91.42	99.62	99.99	100	100	100	100
350	0.12	89.38	99.42	99.98	100	100	100	100
500	0.20	81.95	98.26	99.89	99.99	100	100	100
1000	2.04	13.00	39.52	66.58	84.98	94.36	99.88	99.97

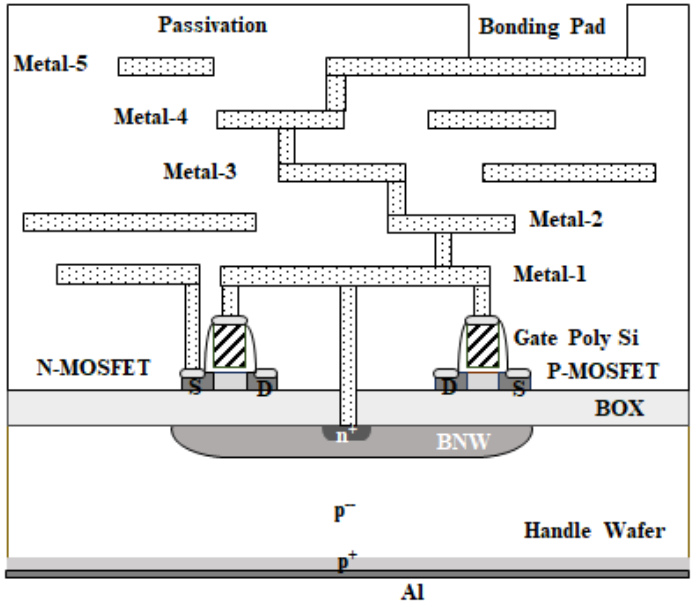
numbers are scaled from study of Mori (Tohoku U, master thesis) made for (5μm)^2 FPCCD, 2014, using Guinea Pig+Mokka

0.75x10^{34}/cm^2/s @0.25TeV?
1.8x10^{34}/cm^2/s @0.5TeV
3.6x10^{34}/cm^2/s @1 TeV

SOI monolithic sensor

Monolithic sensor using silicon-on-insulator (SOI) technology: Lapis 0.20μm FD-SOI
Pixel nodes (in handle Si) are electrically connected to readout circuit (SOI layer) through small vias fabricated in a conventional LSI process.





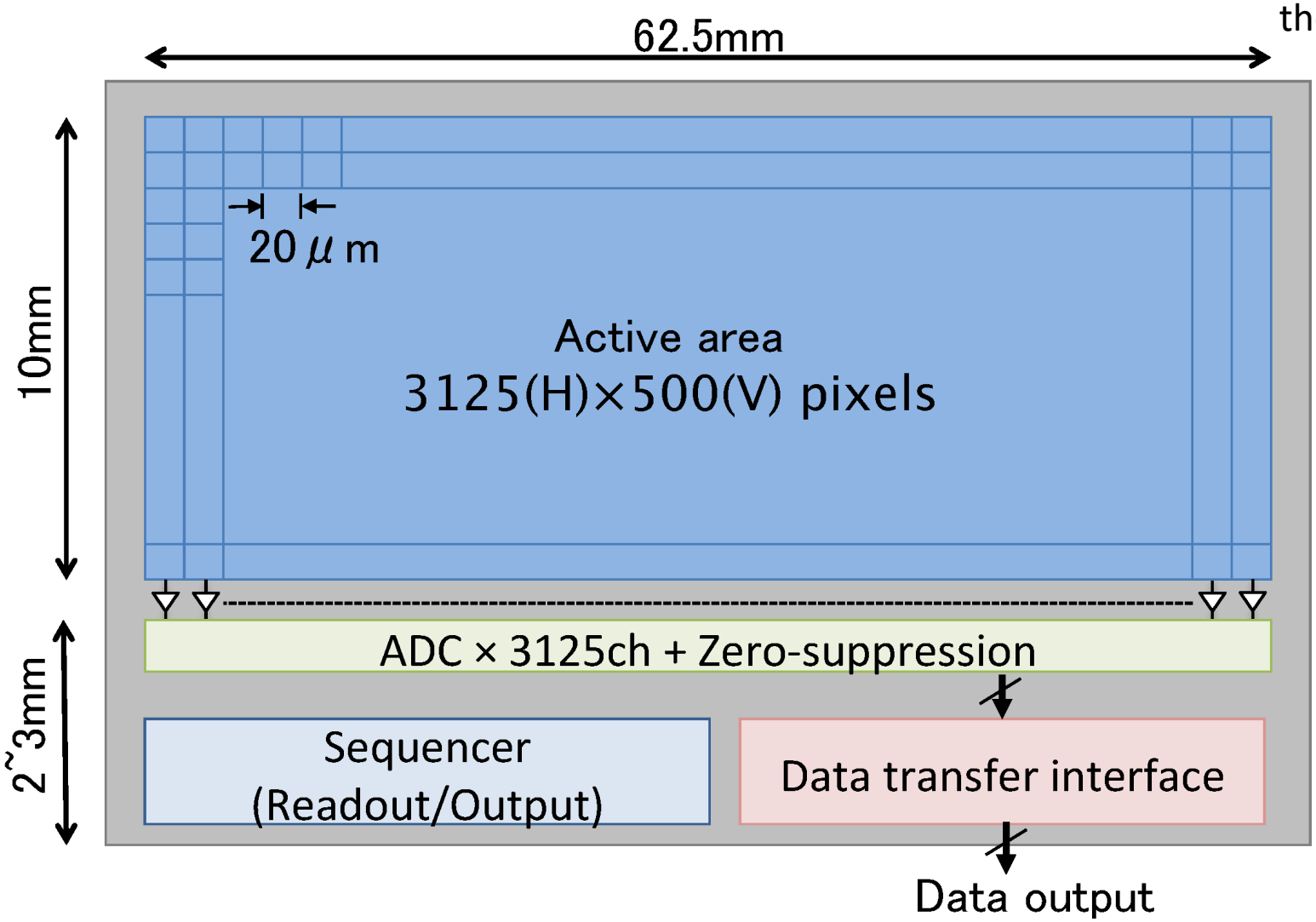
8 μm
MIM cap

50-500 μm
p-Fz, n-Cz

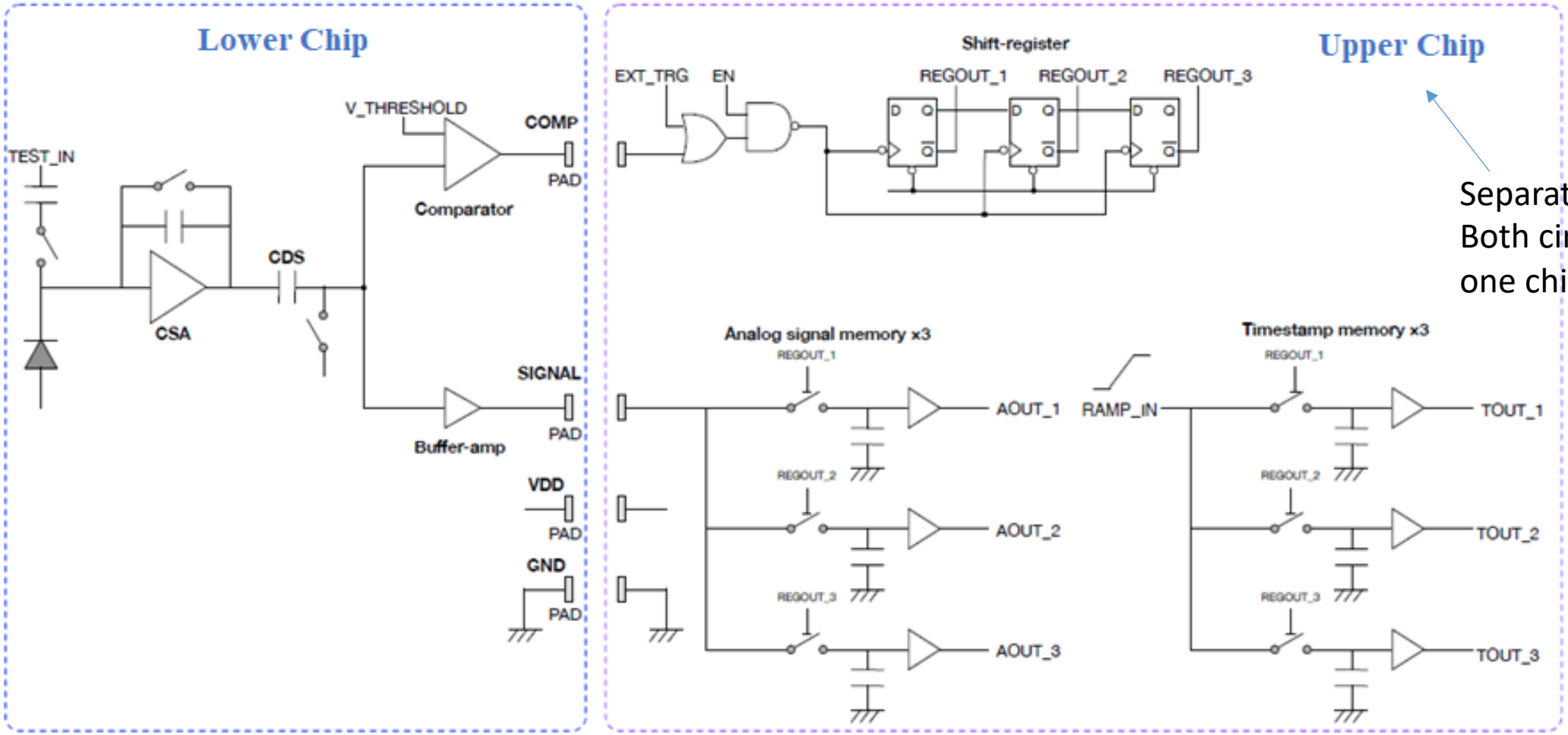
Advantages of SOI Monolithic Sensor
- Bonded wafer (SmartCut™) - sensors can be fully depleted
- Commercial CMOS process is used to fabricate SOI detector
- Extremely Low material budget (can thin down to 50 μm)
- Easy to embed circuits on top of BOX
- Low parasitic capacitance, FETs fully isolated
- Very good compatibility with 3D stacking

SOFIST layout

Ultimate layout to fit in the ILD vertex geometry



SOFIST on-pixel circuit

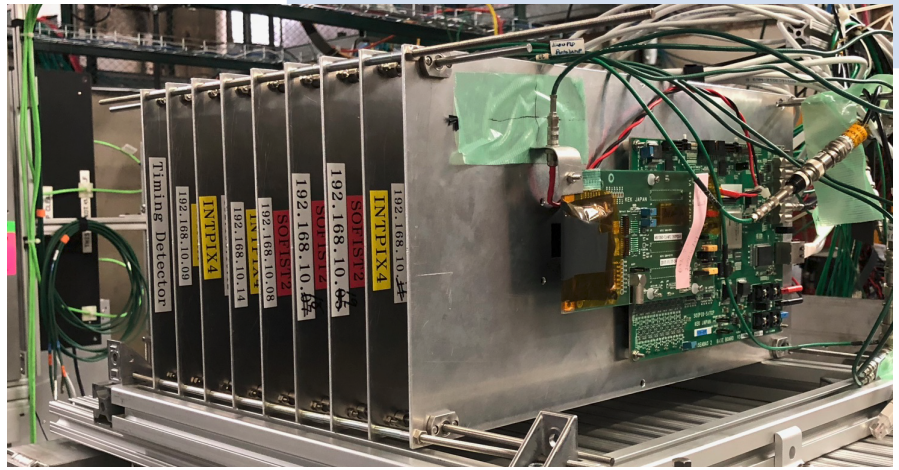


Separation in 3D
Both circuits are in one chip, otherwise

Multiple memories: dead-time less data store possible
Timestamp data: distinguish hits associating to individual events
- separation of beam bunches (554ns) is ideal, but separation O(1us) would help a lot
Readout all memory data (charge and time) in a column by one ADC

SOFIST in development

	Ver. 1	Ver. 2	Ver. 3	Ver. 4
Produced /Tested*	2016/2017	2017/2018	2018/2019	2018/2020
Wafer	SOI	DSOI	DSOI	DSOI
Pixel size (μm x μm)	20x20	25x25	30x30	20x20
#Charge memories	2	0	3	3
#Time stamp memories	0	2	3	3
Chip size (mm x mm x μm^t)	3x3x500	4.5x4.5x75	6x6x300	4.5x4.5x300
Notes	Spatial column ADC	Time column ADC zero-suppr.	Both column ADC	Both** column ADC 3D



* Yearly test beam activities at FNAL
  This year is planned for SOFISTv4

** timestamp function is not testable due to mis-match of the readout and sensor wafer types

SOFIST-v1 spatial resolution

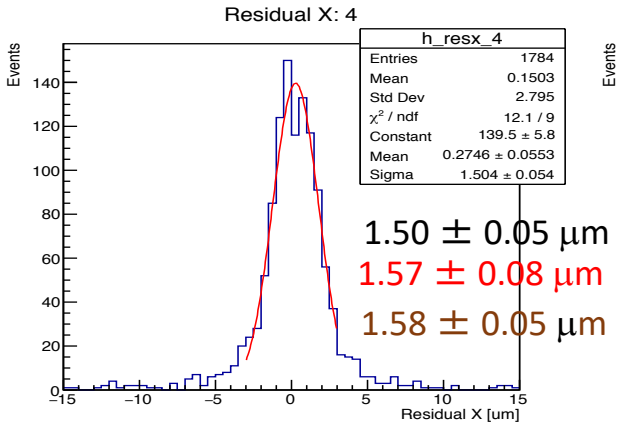
SOFIST residual to FPIX track (σ_track~0.57/0.65μm)
Bias=130V (~500um depletion) =>15V (~200μm depletion)
Readout: external 12-b ADCs =>on-chip 8-b column ADCs

20x20μm pixels

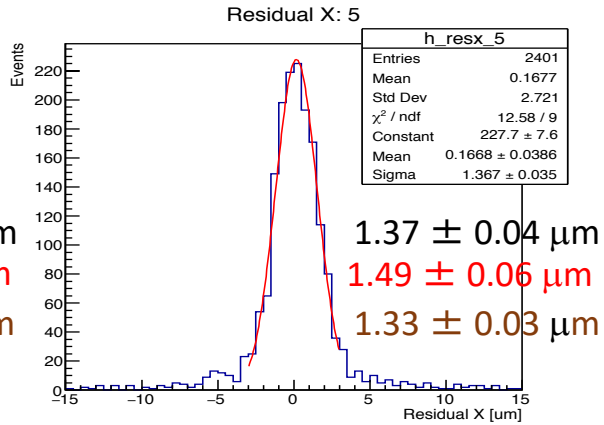
plots are for "black case"

SOFIST#1(BPW14x14) SOFIST#2(BPW16x16)

Residual X

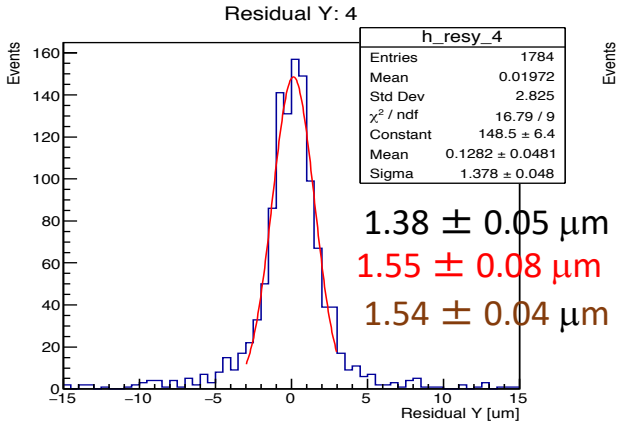


1.50 ± 0.05 μm
1.57 ± 0.08 μm
1.58 ± 0.05 μm

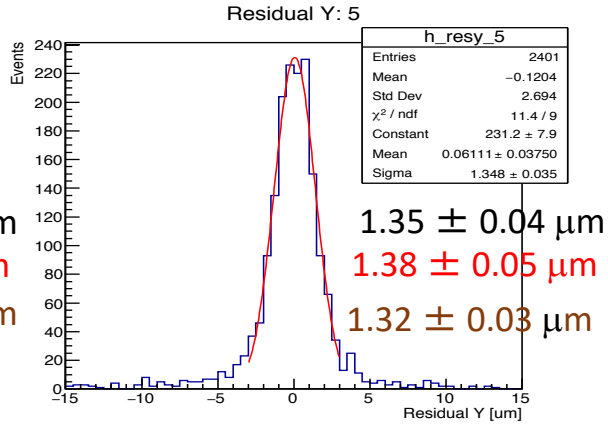


1.37 ± 0.04 μm
1.49 ± 0.06 μm
1.33 ± 0.03 μm

Residual Y



1.38 ± 0.05 μm
1.55 ± 0.08 μm
1.54 ± 0.04 μm

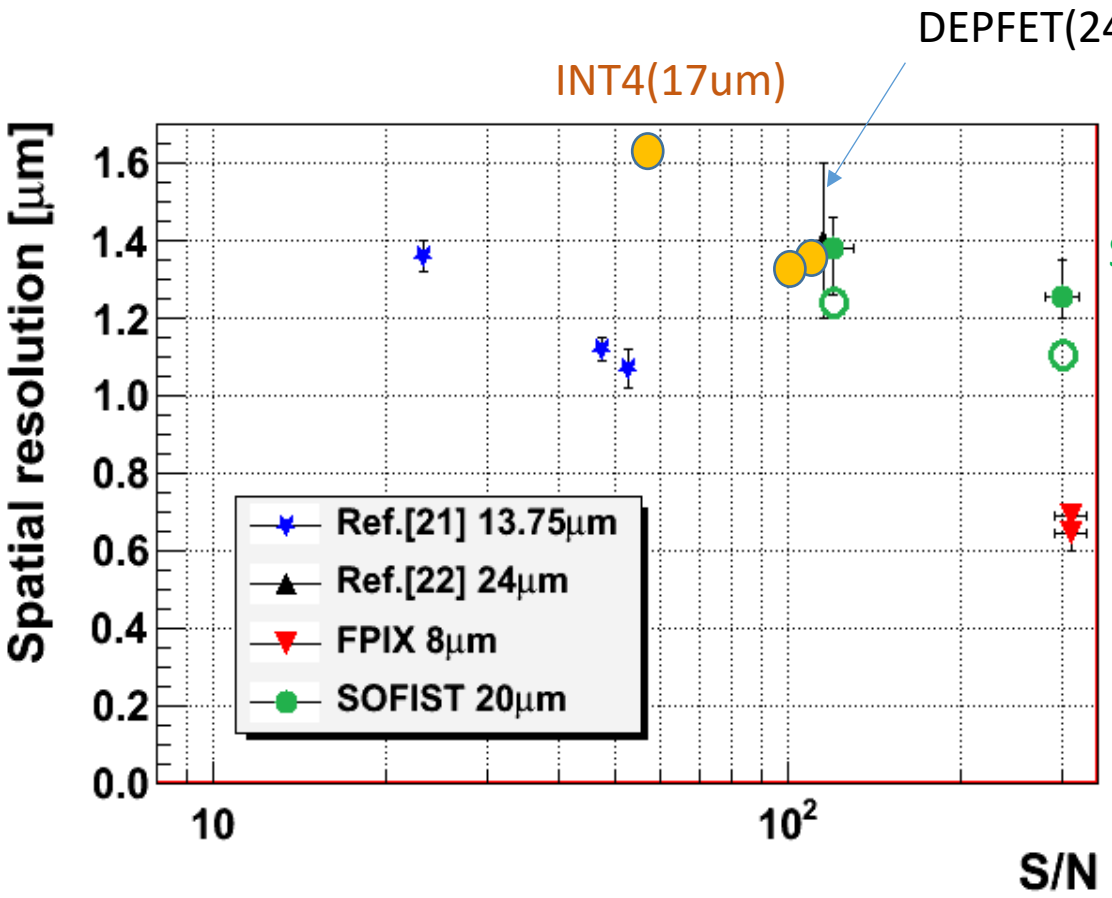


1.35 ± 0.04 μm
1.38 ± 0.05 μm
1.32 ± 0.03 μm

S/N~300 (130V)
~120 (15V)

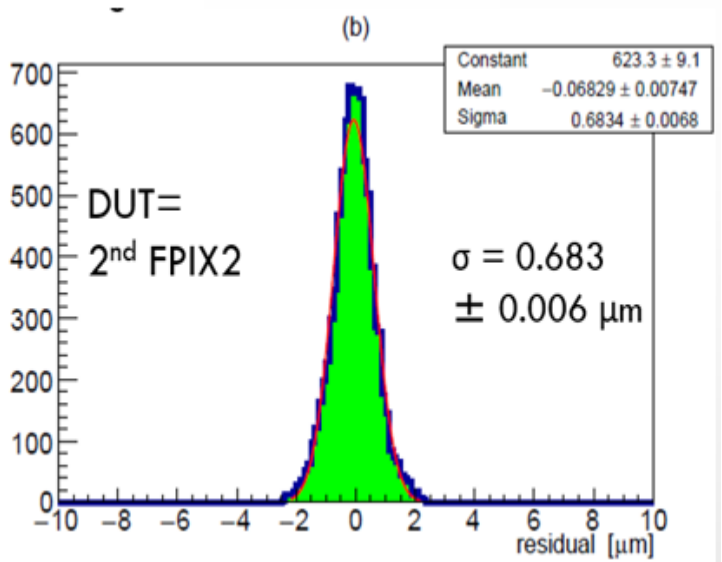
Sensors with O(1um) spatial resolutions

Spatial resolution improves with S/N as charge-weighted mean position calculation
Mostly SOI sensors in this competition
World record is 0.65μm achieved by FPIX 8um



SOFISTv1 (20um)
tracking error subtracted
η correction (calculation)

FPIX (8um)

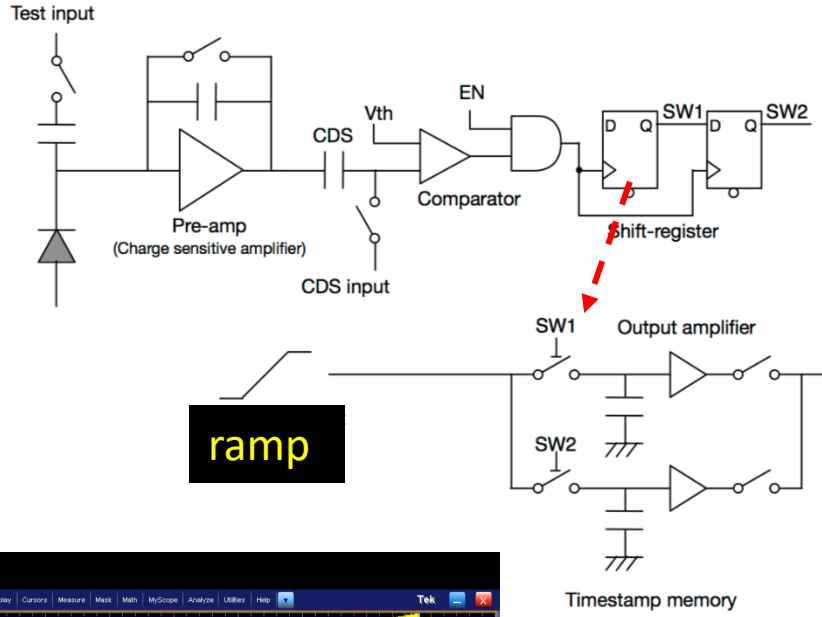


FPIX residuals including tracking error
K. Hara et al., PoS(Vertex 2017)035 pdf

25x25μm pixels

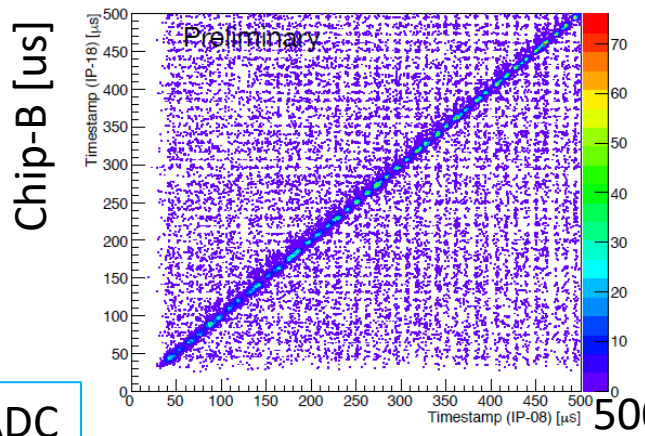
SOFIST-2 Time stamp resolution

SOFISTv2 for timing study thinned to 75 um

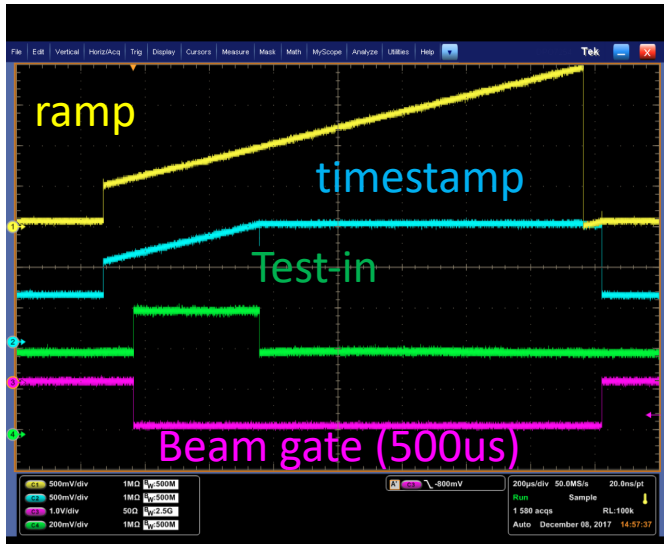


ext. 12-b ADC

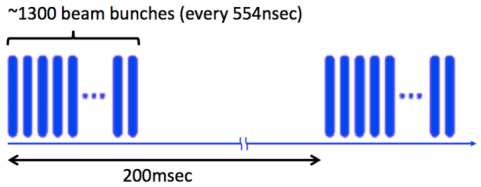
Timestamp correlation of two sensors in a beam



Combinatorial background due to other particles in the same beam gate



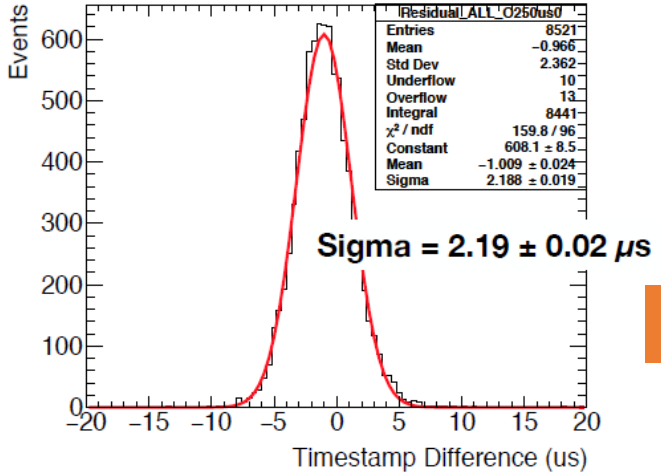
Beam gate(500us) simulates the ILC beam train



ILC beam structure

タイムスタンプの分解能

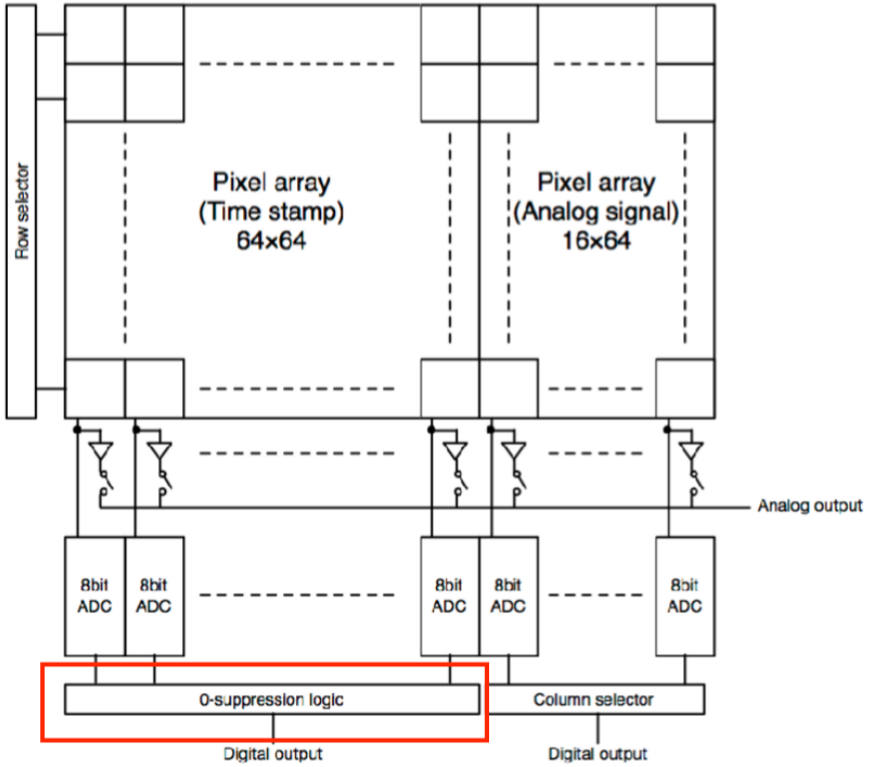
SOFIST ver.2 #1 and #2

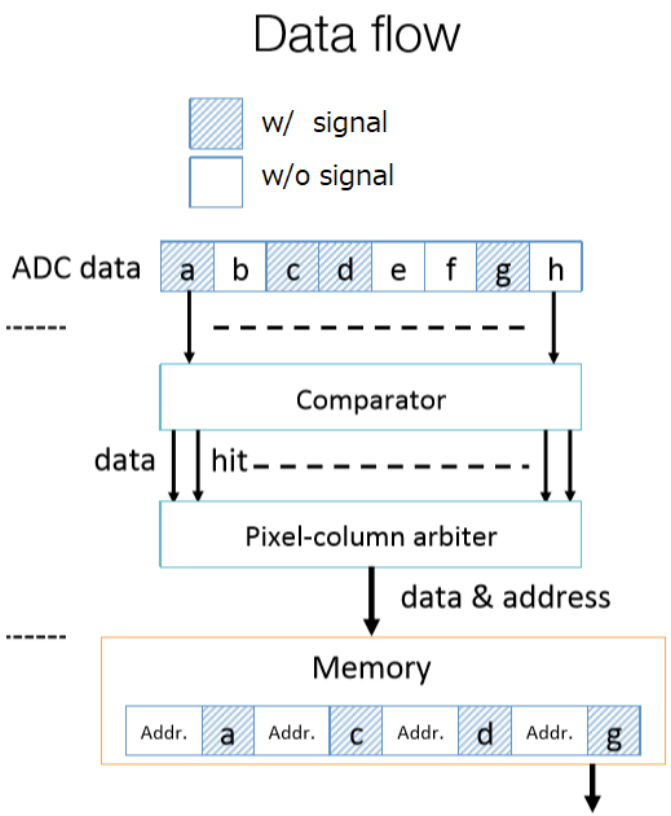


σ=1.55us

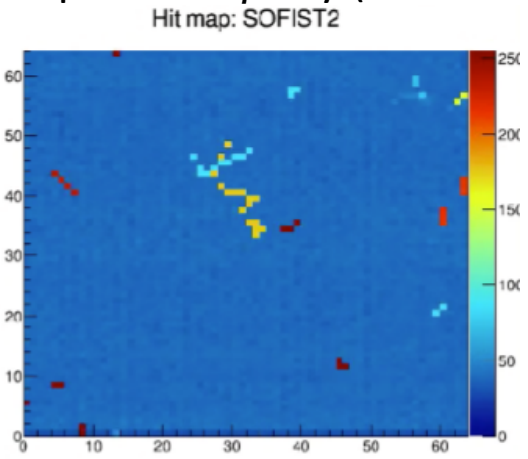
Intrinsic resolution: 2.19/√2 ~ 1.55 μs

SOFIST-2 zero-suppression logic

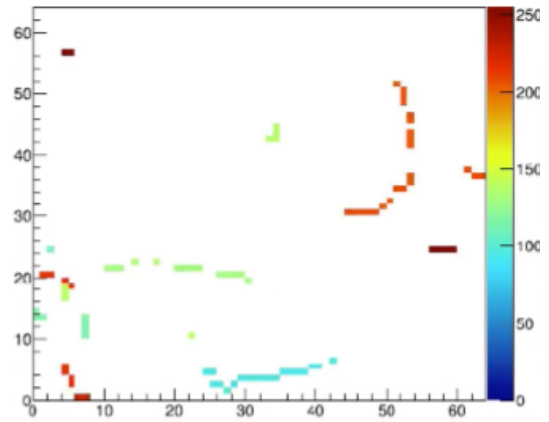




Response to β-ray (time data)



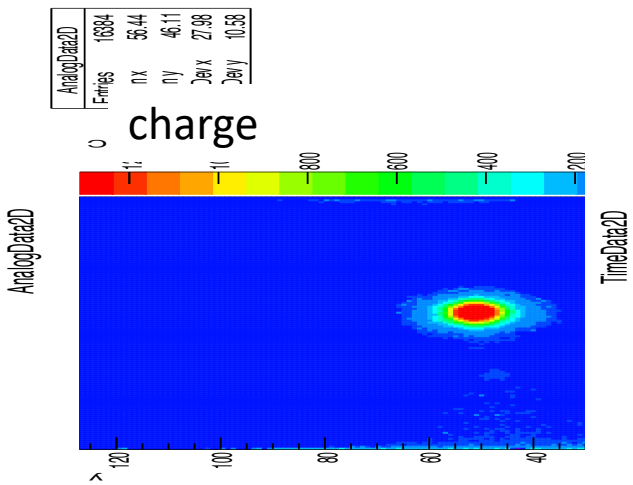
full scan

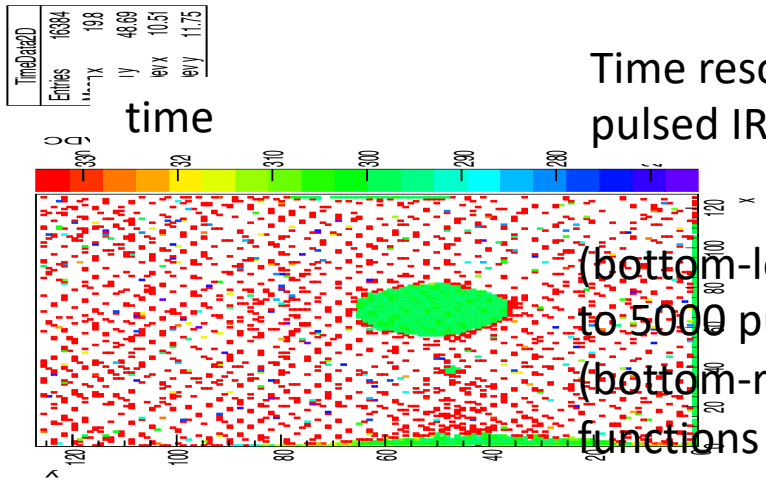


Zero-suppr. (whites are not R/O)

Digitised column data are examined and only hit pixels are stored in FIFO
Total scan time= AD conv. ~5 us/colmn(64) x columns(64)~320us
vs 340us measured @25MHz clock

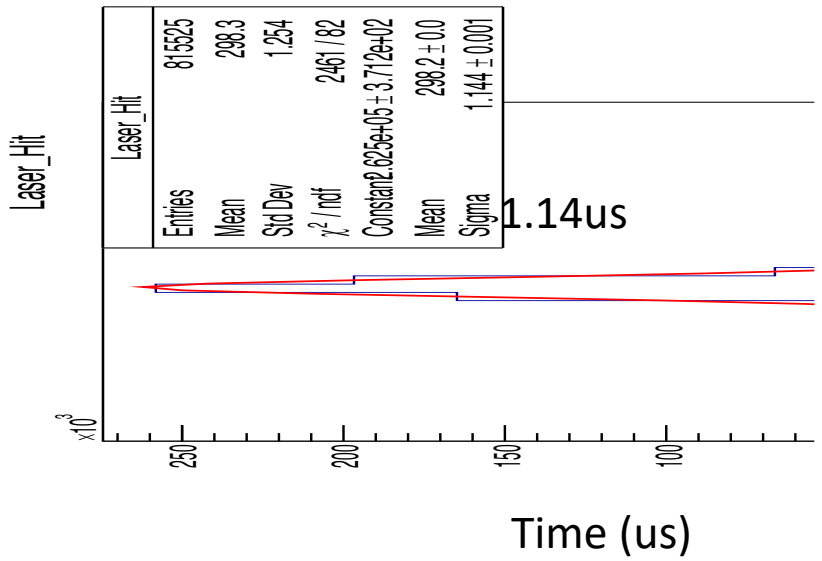
SOFIST-3: time resolution w/ laser

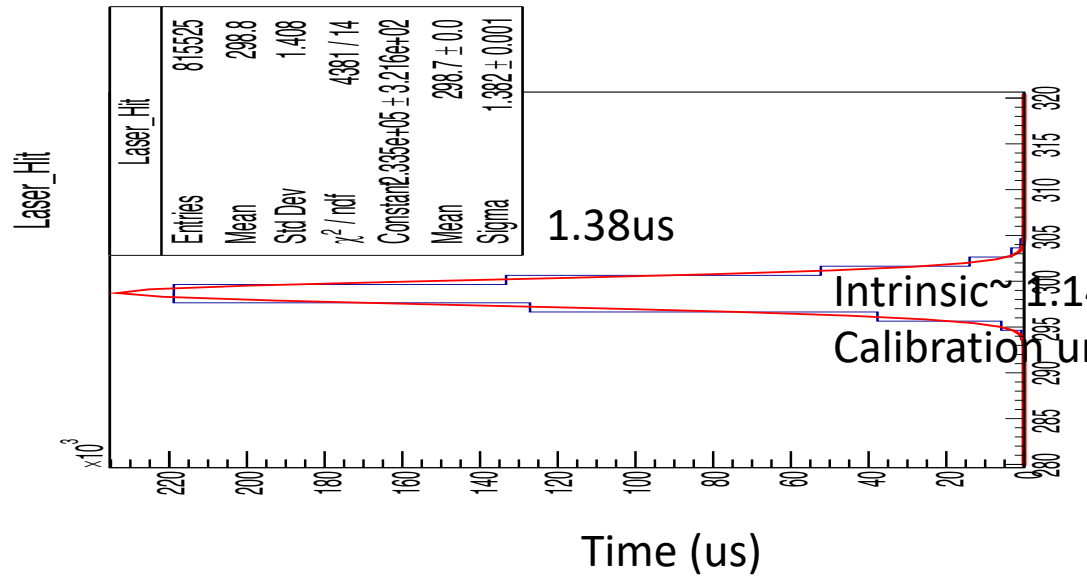




Time resolution of SOFISTv3 was investigated by injecting pulsed IR laser with fixed delay times

(bottom-left) Repeatability of the ADCs (converted to us) to 5000 pulses for all the illuminated pixels
(bottom-right) Same but calibrations using simple linear functions was used for ADC to time conversion

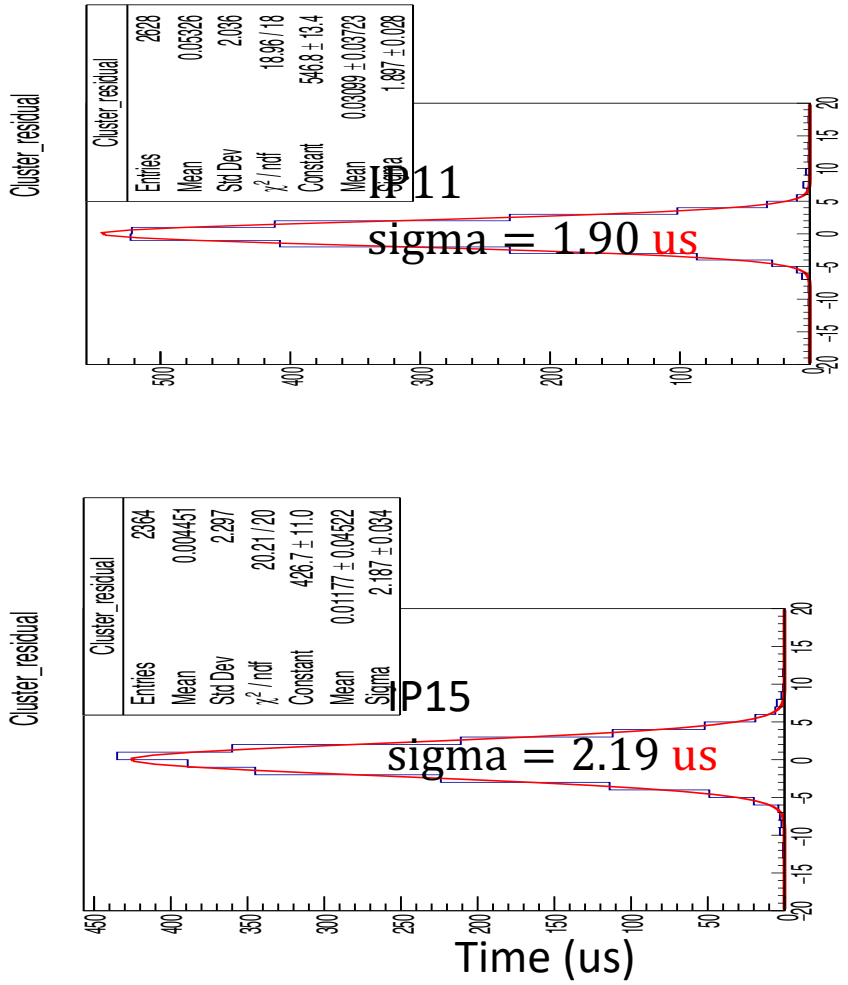




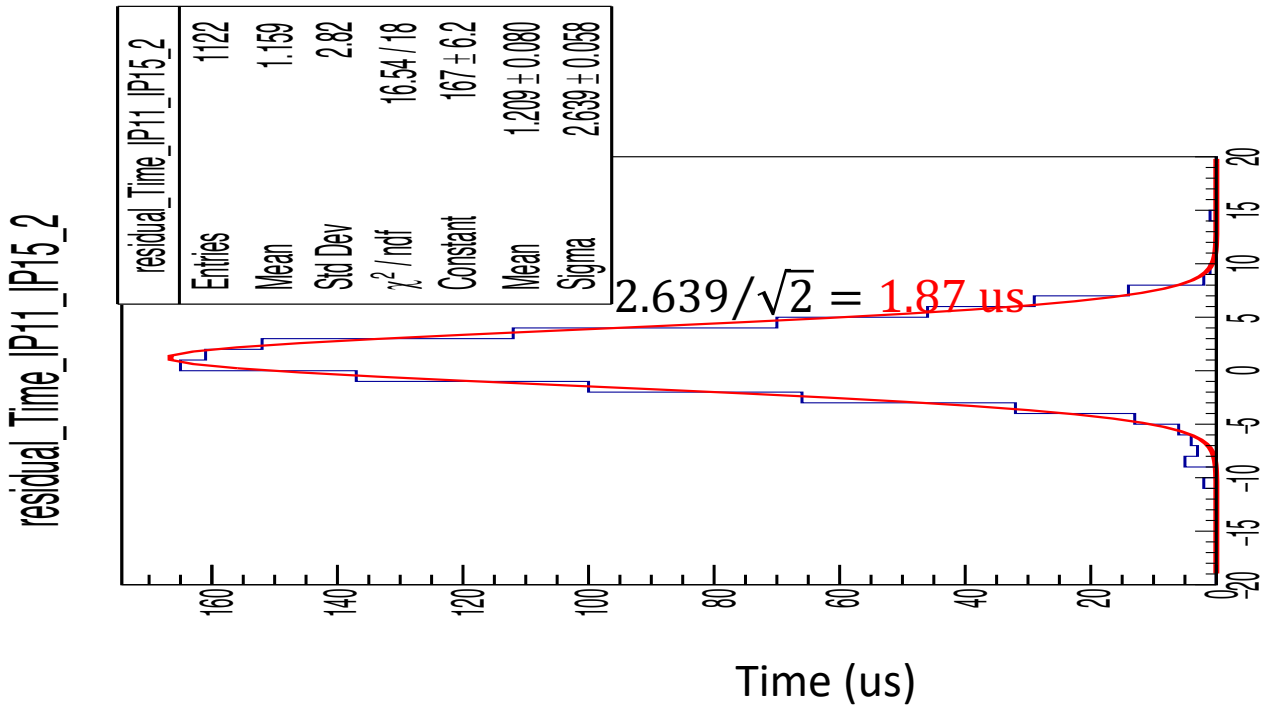
Intrinsic~ 1.14 us
Calibration uncertainty~0.8us

SOFIST-3: time resolution in TB

Time resolution of SOFISTv3 evaluated from time difference of two sensors



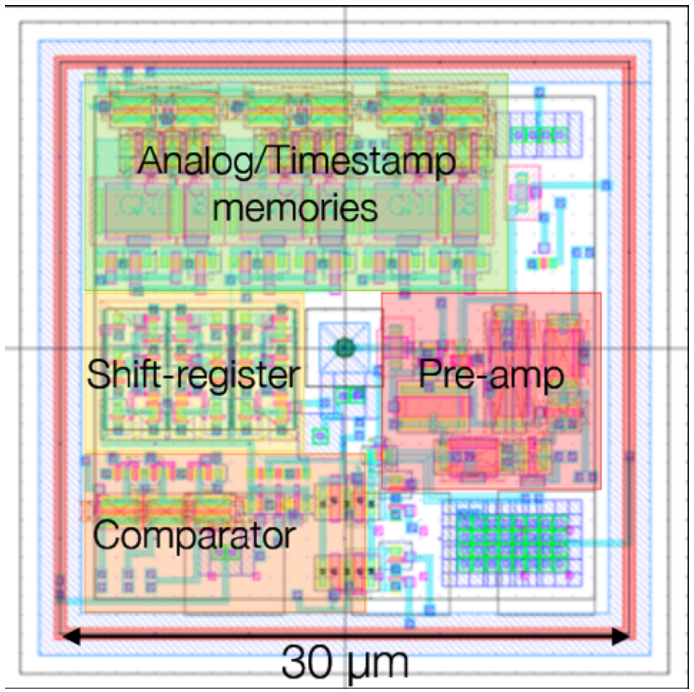
2hit clusters: time difference



Time resolution <2us is demonstrated from test beam data

SOFIST-4: 1st 3D stacked SOIPIX sensor

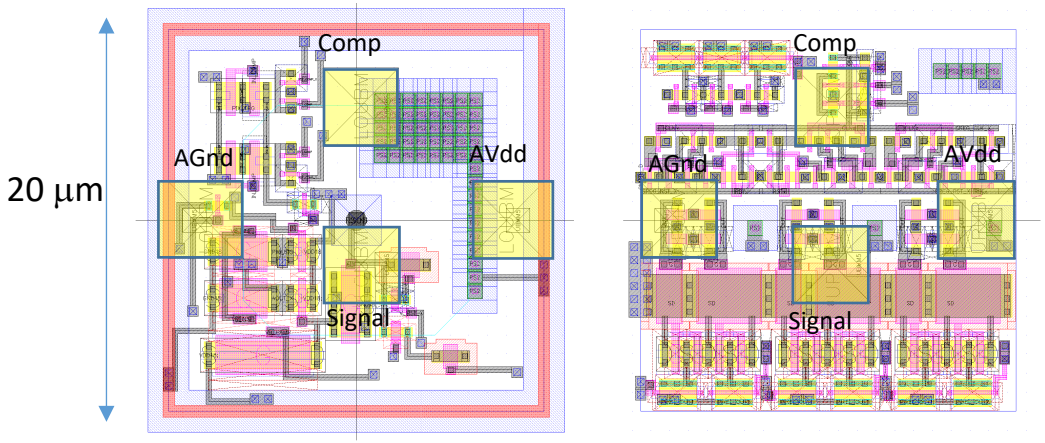
SOFIST Ver. 3



SOFIST Ver. 4

Lower chip

Upper chip

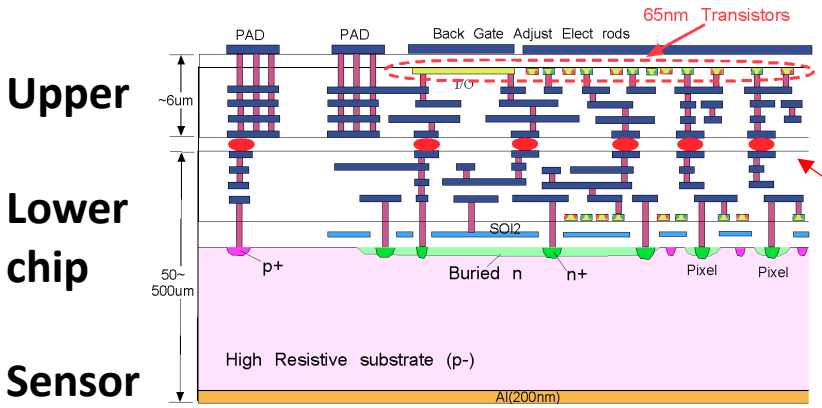


Beam-tested and under final evaluation

SOFIST-4 3D stacking

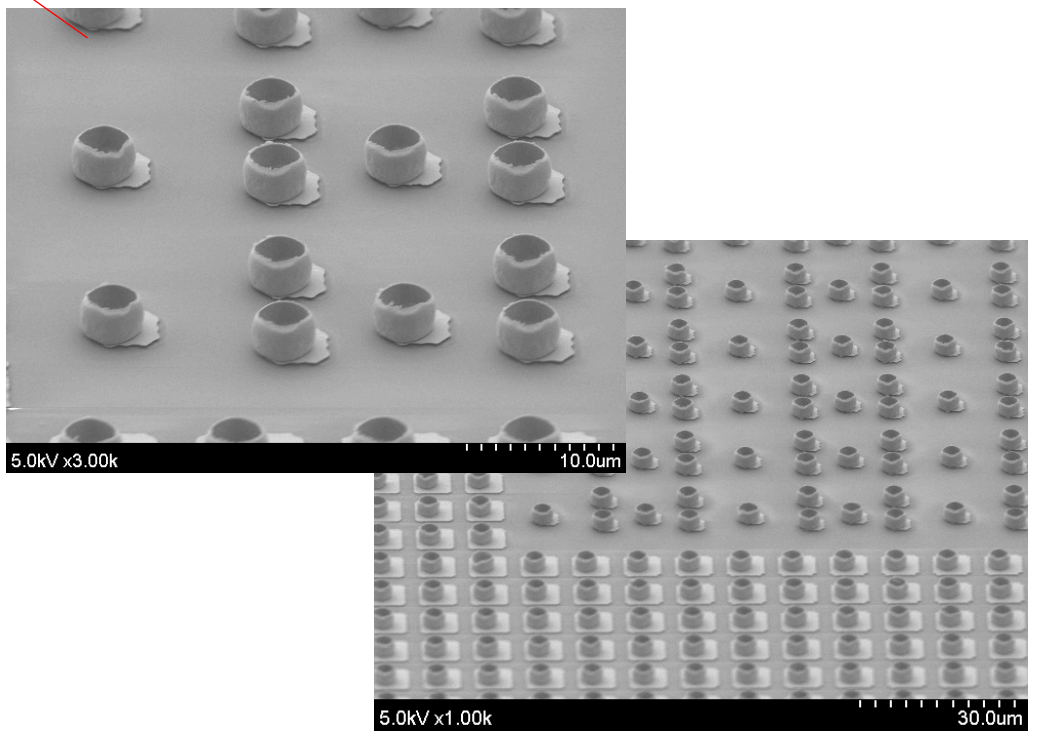
3D stacking of SOI chips (chip-on-chip)

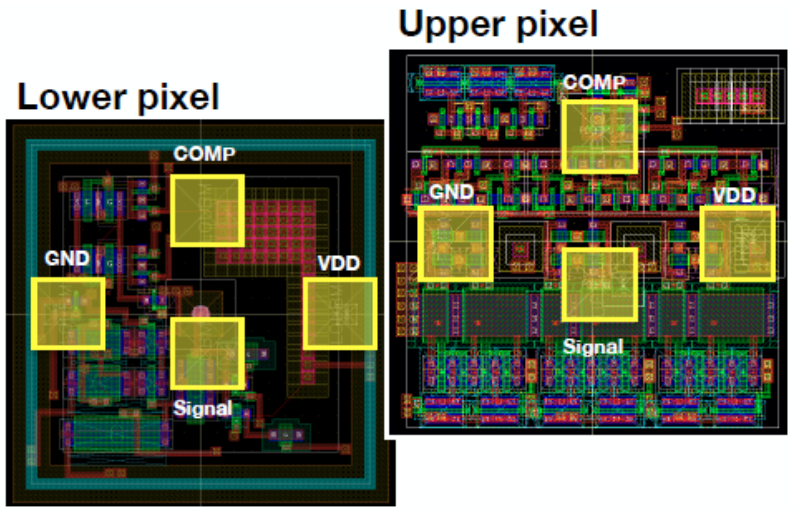
→Electronics circuits in two chips are fused using cylindrical micro-bumps to extend the circuit functionality in limited space



Tohoku MicroTech

Pixel size: 20 x 20 μm
Under bump metal: 4 x 4 μm
Cylinder bump: 3 μmϕ





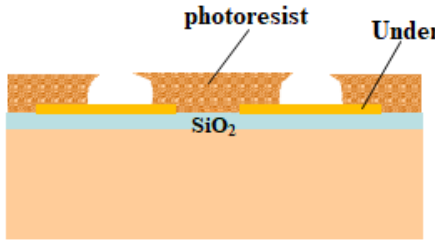
2 bumps + 2/2 for power&return

Process flow of Au cylindrical bump

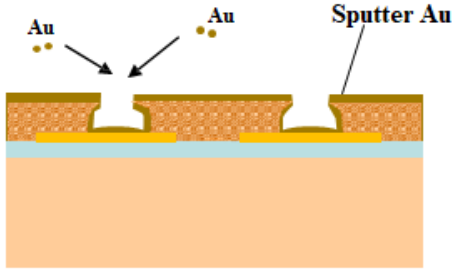
Key Technology : inverse-tapered photoresist & low incident-angle Au sputtering

Processed by T-Micro

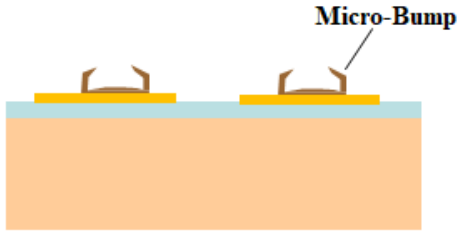
Bump Hole Patterning

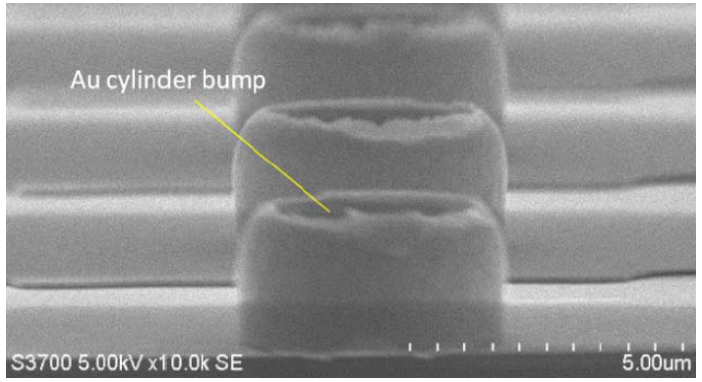


Low incident angled Au Sputtering

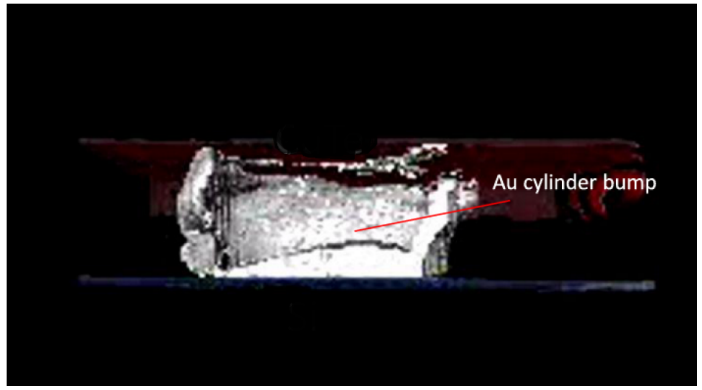


Resist Lift-off



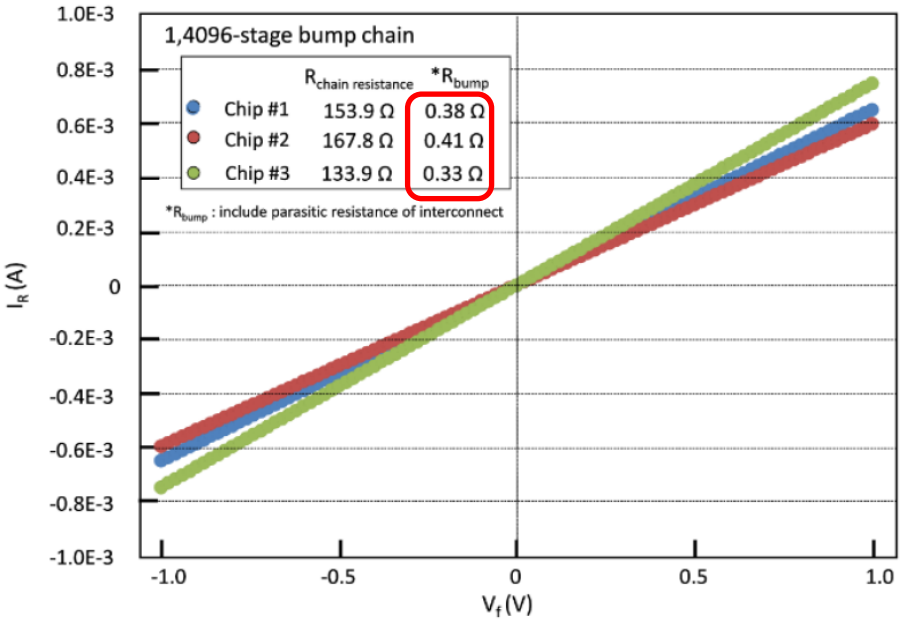


Au Cone Shape Bump



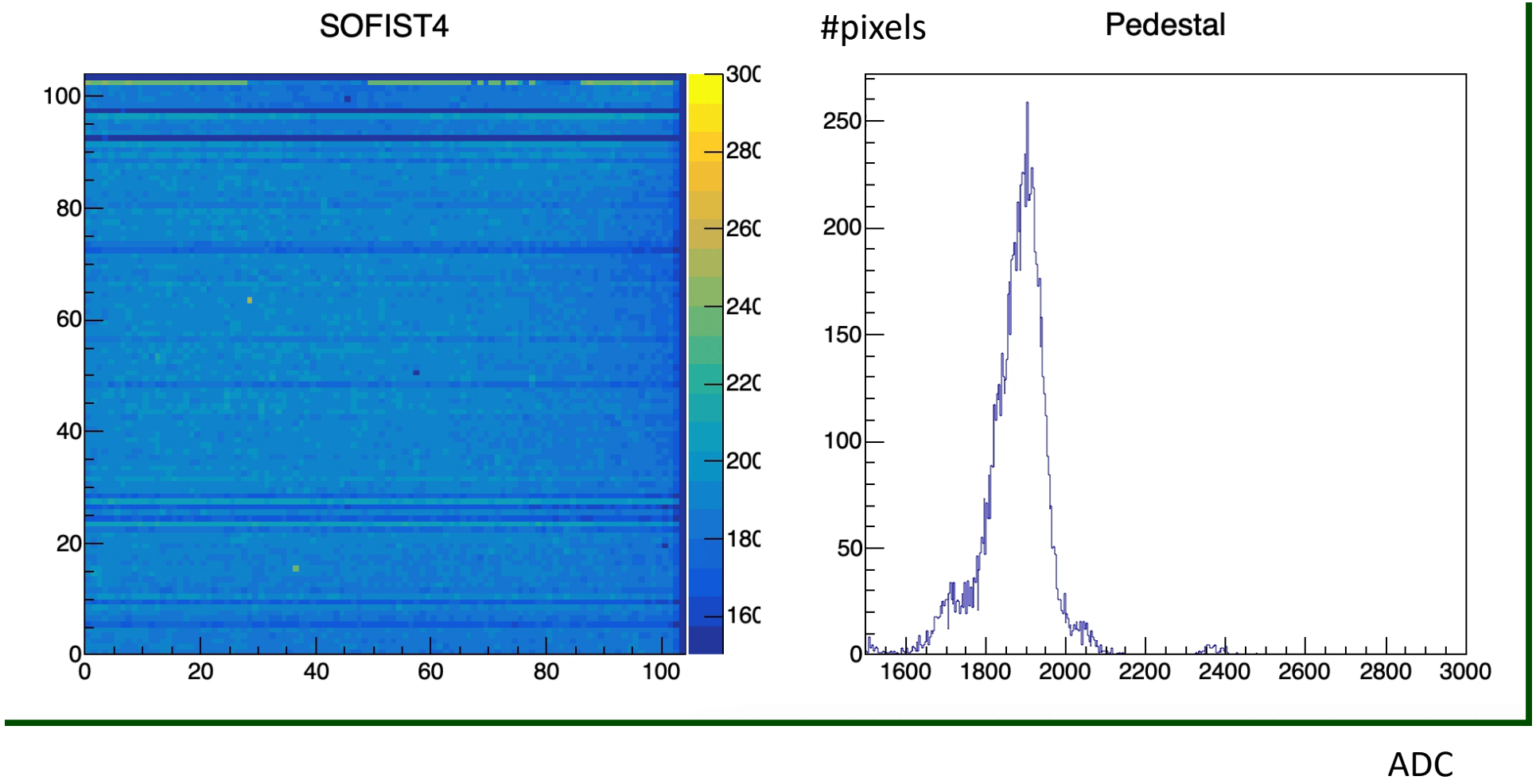
Cross section of junction

Bump Resistance



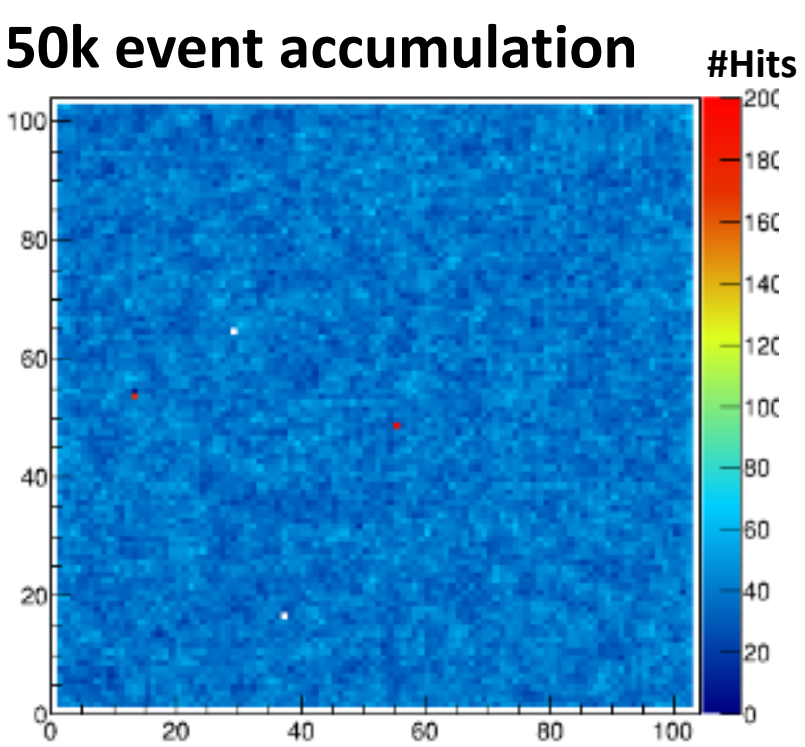
0.3~0.4Ω/connection

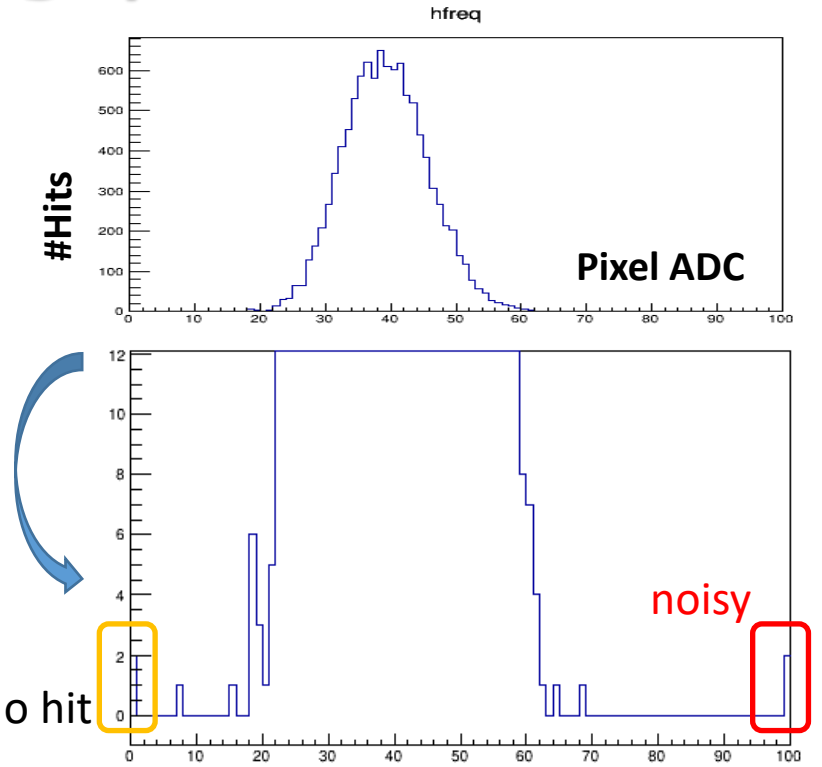
Response to β source



μ-bond yield by β source

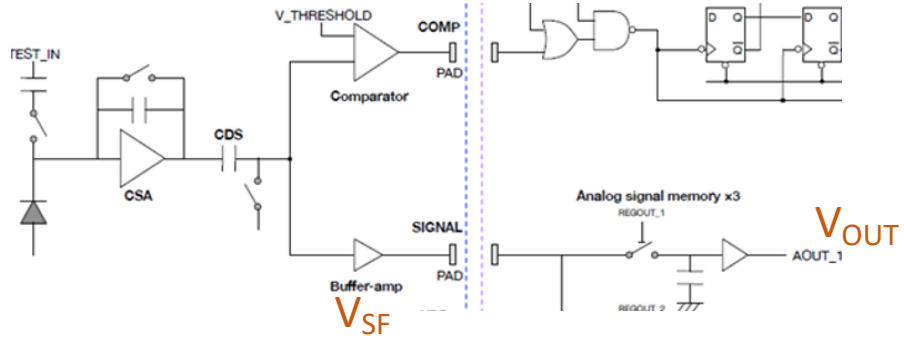
50k event accumulation

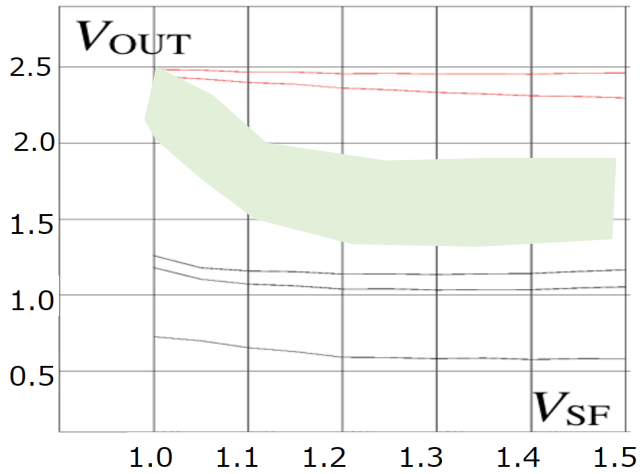




 # bond failures : (2~4) of 102 × 102

$$good\ bonds \sim 99.96\%$$





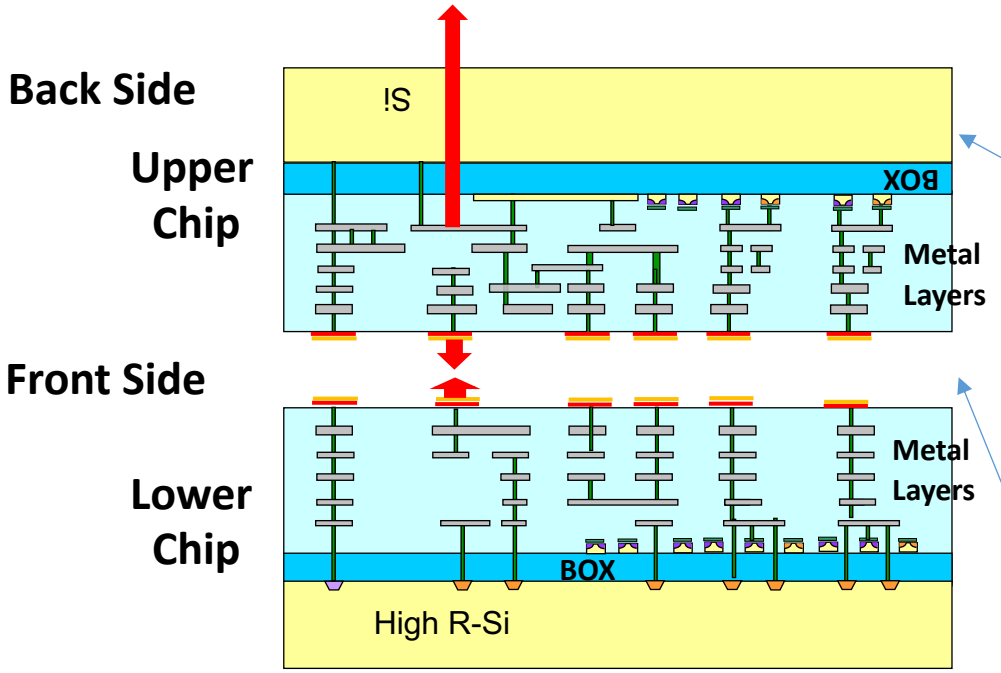
Bump bond failure

Genuine channels

Preamp failure

Concepts for chip-on-chip connections

In the case of SOI chips …



Etch down Si and pads are placed for WB: Relatively thick (150-200nm) BOX of Lapis helps terminate etching as required

Inject epoxy for reinforcement

Note: Renesas' 65 nm TB-SOI and ST's 28 nm TB-SOI also utilize "through BOX via" technology

Typical concepts for electrical connections between front and back sides

Back Side

Through Silicon Via (TSV)
size ~5 μm, complicated

Through BOX Via (TBV) Our technology
size ~0.3 μm, simple

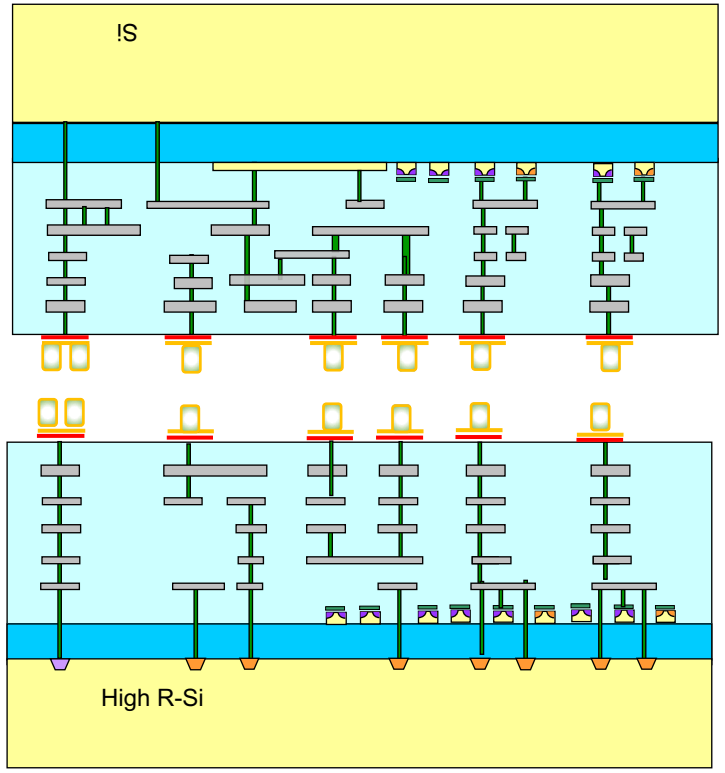
Front Side

Cu-Cu direct bonding (SAB)
require quite flat surface

μ-Bump **Cu/Ni/SnAg**
In
Au (cone, cylinder)
oxidation-resistant metal

Advantages of SOI micro-bump bonding

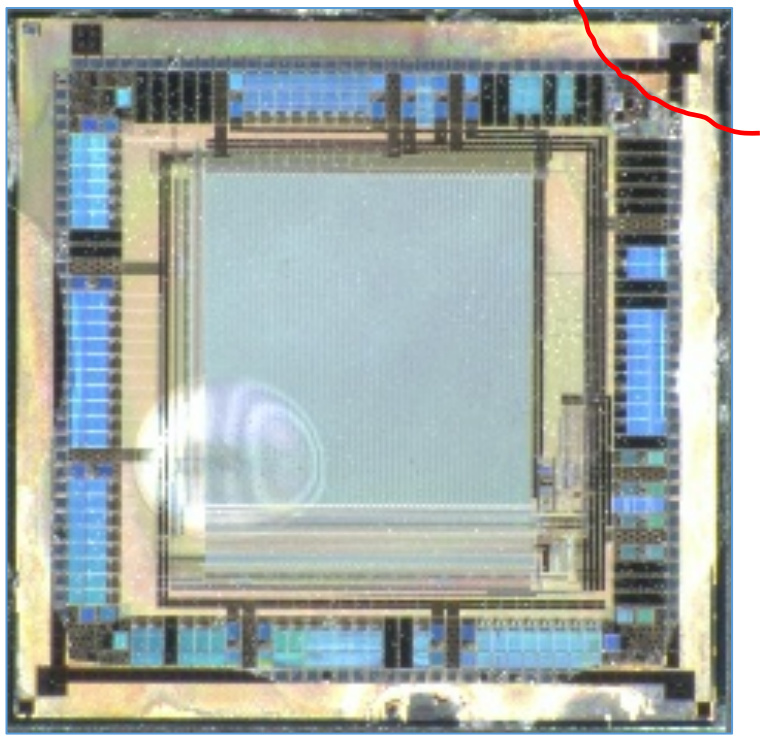
- Requirement on the surface flatness is moderate, as the height of the cylinders can be self adjusted by deformation: a few μm tolerance. cf. Cu-on-CU 3D
- Soft cylindrical gold bumps result in high-connection yield, as shown.
- No TSV , but Through BOX via (TVB) are processed in the SOI CMOS circuit processes. Fine TVB (0.3um) can be fabricated.. cf. TSV 3D
- Relatively thick BOX (150-200nm) easies top silicon removal etching process
- Upper chip: Only CMOS circuit below SiO_2 remains.
  - The remaining thickness is about 8 μm.
- Circuit chip has SiO_2 layers on both sides: stacking can be further repeated



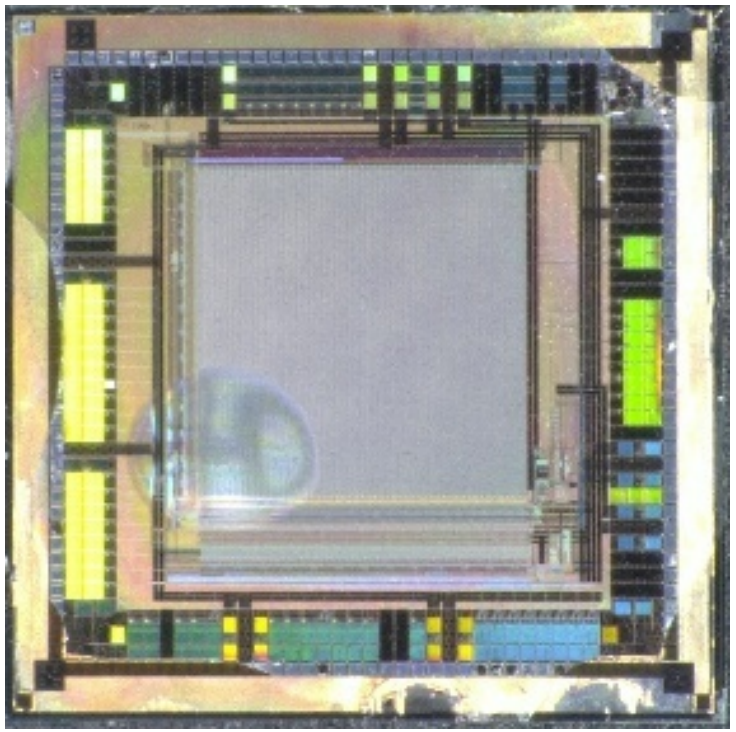
SOI and 3D are in very good compatibility

Rad-hardness of adhesive glue

Upper Chip Peeled Portion



Proton irradiation : 400 kGy
(5×10^{14} cm^{-2} in 1 MeV neutron equivalent)



Before irradiation

After irradiation

No obvious damage was observed

even though the dose level is threshold to create Si displacement defects.

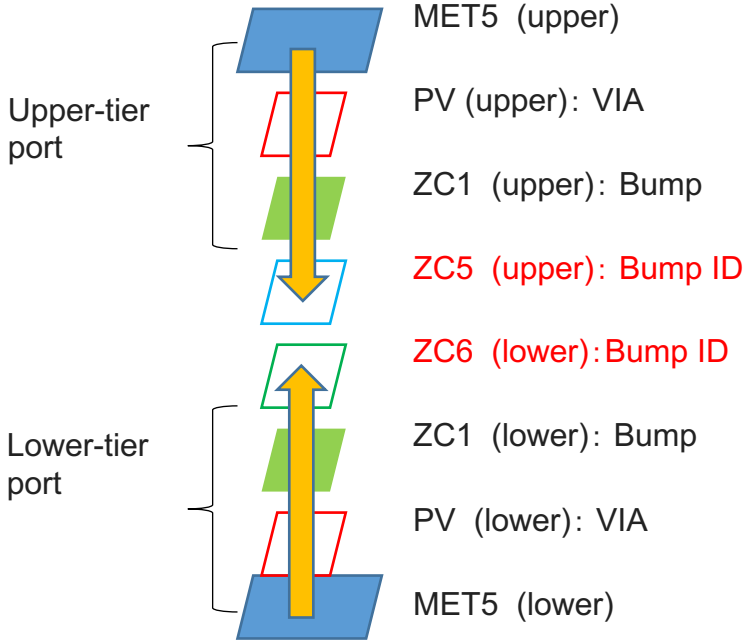
An test chip from process condition tuning was evaluated. The upper chip had some peeled edges but still good enough to evaluate glue damage.

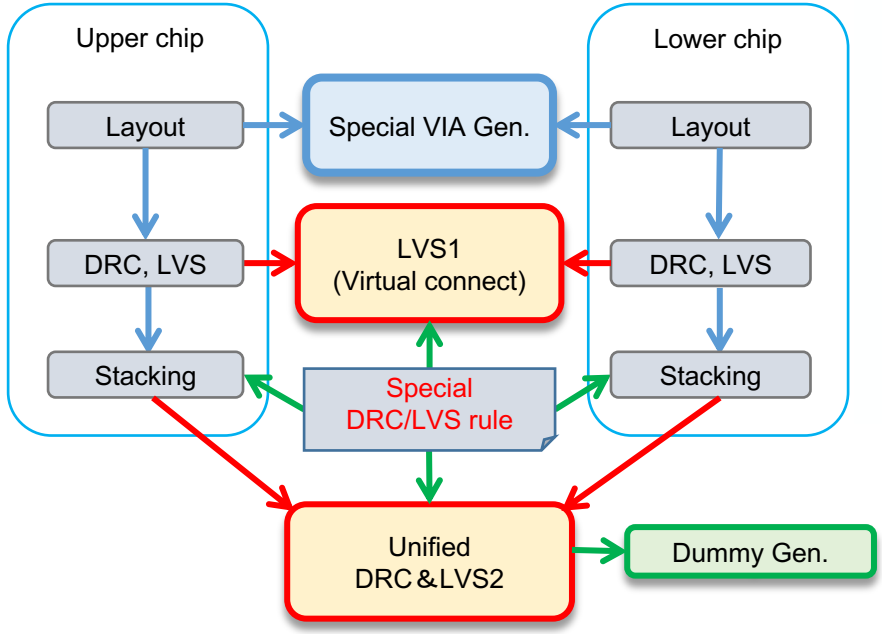
- Color difference is due to lighting

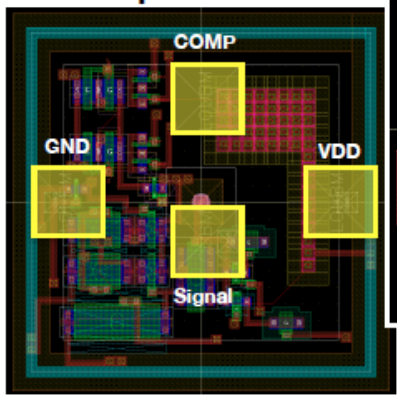
3D design tool

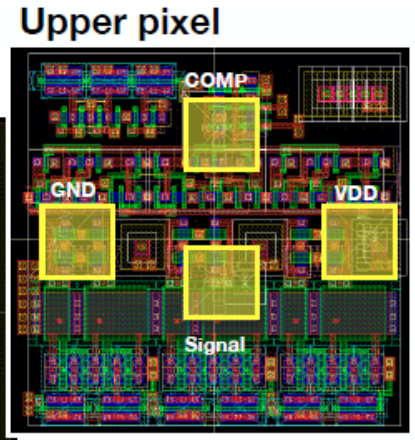
- *Virtuoso* with dedicated rule files.
- Virtual layers are automatically generated between upper and lower chips that unify the chips geometrically and logically.
- *DRC* (design rule check) and *LVS* (layout versus schematic) can be applied for the whole pixel system.

3D can be designed as for conventional SOI









Summary

- In the past 7 years, we have been developing SOFIST for the ILC vertex tracker
- Excellent performance has been demonstrated on the spatial and timestamp resolutions, verifying superiority of SOFIST as a deadtime-less device recording timestamp at O(1us) precision over the ILC train duration. Column ADCs, sensor thinning to 50um have also been verified.
- 3D stacking allows to keep the pixel size small (20x20um). SOI is in very good compatibility to the 3D stacking.

However, to adopt SOFIST to the ILC vertex

- Power consumption needs to be lowered. As the demonstrated detector performance is well within the requirements, compromise of the preamplifier speed (hence power) is foreseen.
- Periphery circuits to analog power-off in between trains, to transfer digitized data, and etc., with micro-channel cooling incorporated are to be investigated.
- have a full size chip

Acknowledgements:

JSPS Grant-in-Aid for Scientific Research on Innovative Areas (No. 25109006) 2013-2017

Japan/US Cooperation Program in the Field of High Energy Physics 2016, 2018-2019

FTBF- FNAL test beam facility

CYRIC (Tohoku U) for proton irradiation

VDEC (U Tokyo) in collaboration with Synopsys, Inc., Cadence Design Systems, Inc., and Mentor Graphics, Inc.

Lapis is the closest foundry to ILC
T-Micro is in Sendai
Proton irradiation at Tohoku U

https://mapandnews-japan.com/mapsearch_touhoku.html

Backup

Power dissipation

Current SOFIST: preamp + NMOS SFs: (2.75 uA) x 64 x 64 pixels x 1.8 V ~ 13mW ⇒0.86W/full chip⇒126W/146chips
or 138mW/cm^2

We started investigating ALPIDE type low power preamp*

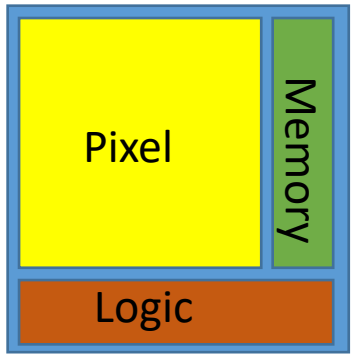
*Comparison of preamp characteristics		
Parameters	SOFIST	ALPIDE for SOI*
Preamp Gain	40 µV/e-	~4 mV/e$^-$
Sensor capacitance	34 fF	3 fF
Pixel power	2.75 µA/cell	80 nA/cell
	*50um depletion	*i_reset 0.2nA

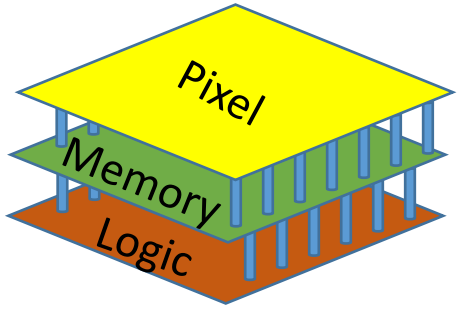
From TDR

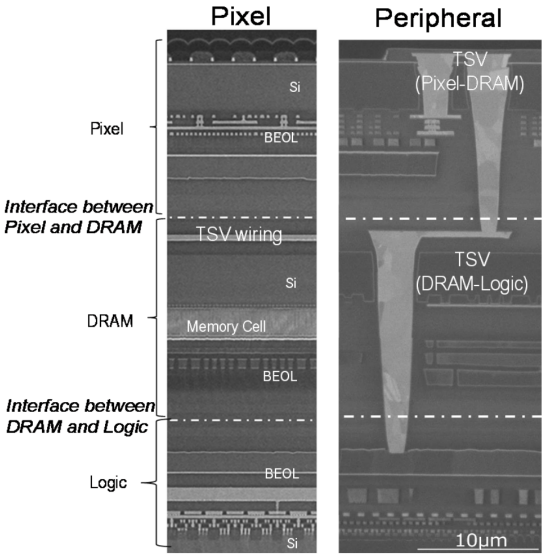
CMOS 600W⇒10W by 2% duty cycle – air cooling
FPCCD 35W inside the cryostat (50um CFRP sheets) – two-phase CO2 cooling
DEPFET – air cooling
For 10W for the entire barrel（S~1600cm^2) ⇒6.3mW/cm^2 ?

3D stacking (1) TSV

- For the commercial image sensors, the first trial is to move the peripheral circuits to the second chip and stacked by using TSV, through silicon via.



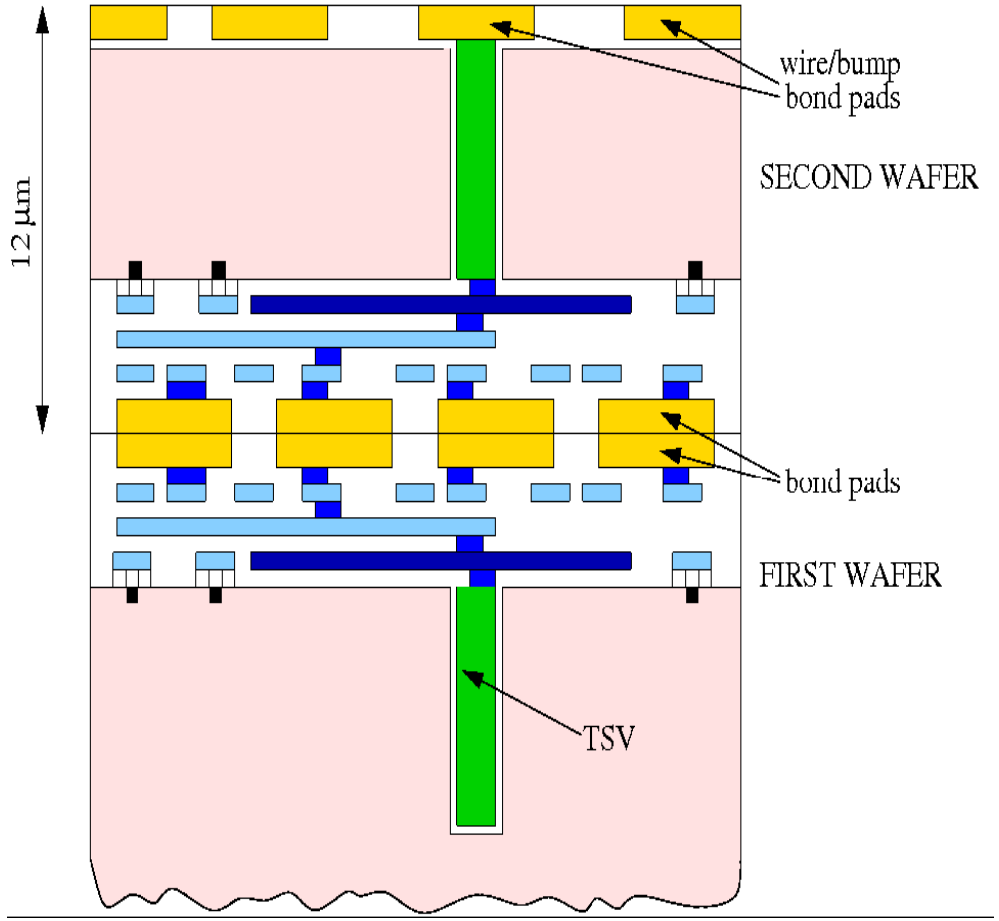




- This is not an answer for HEP. We have to increase the performance of circuit in each pixel. Pixel-by-pixel connection is necessary.
  - Parallel data processing.
  - Low power operation thanks to minimum parasitic capacitance.

3D stacking methods (2)
Direct Bonding Interconnect

- Two wafers are prepared.
- The bonding surface is flattened and cleaned.
- Aligned and attached. Apply suitable pressure and heat for the diffusion bonding of pads.
- SiO2 surfaces is also fused, resulting in the stable structure.
- Widely used for the mass production of high-end image sensors.



From the slide of Valerio Re, Vertex2018