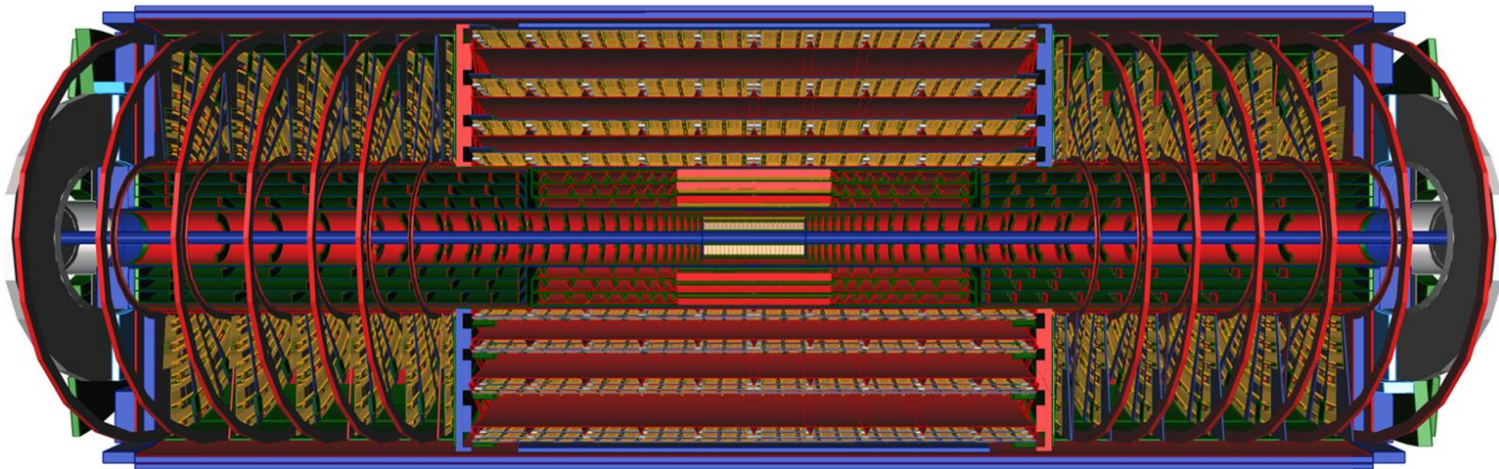
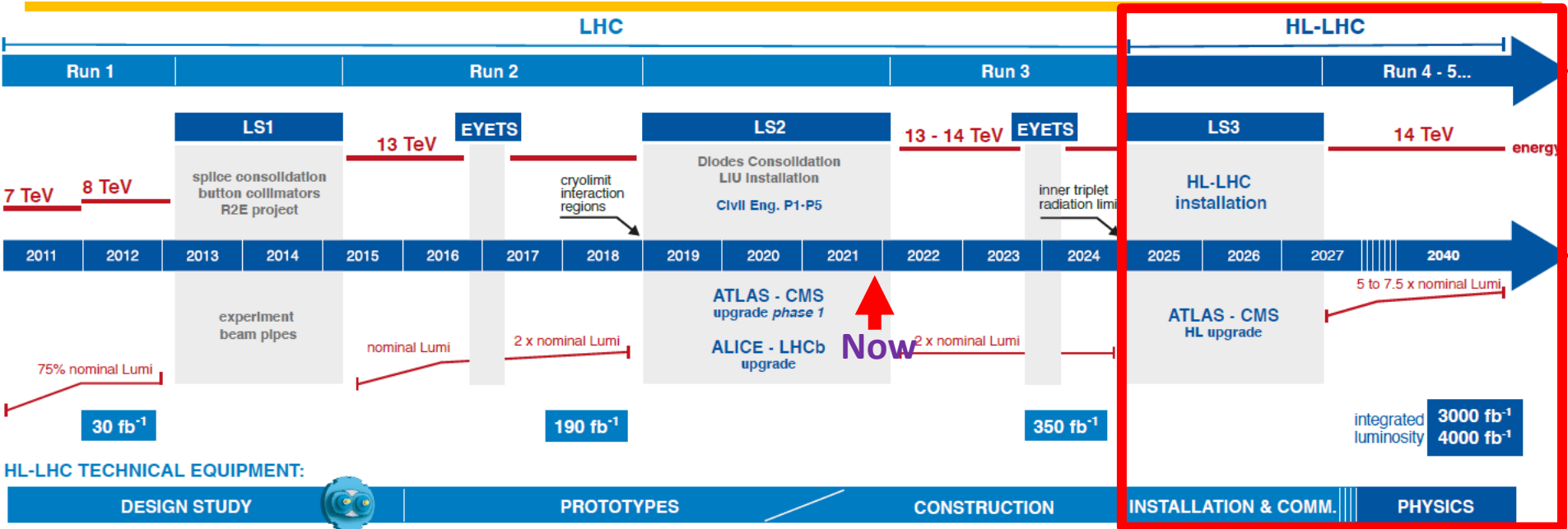


Design and Construction of Pixel Detectors for the ATLAS ITk at HL-LHC

Koji Nakamura (KEK) on behalf of ATLAS group



High Luminosity LHC (HL-LHC)



- High Luminosity LHC (HL-LHC) start in 2027 to take 10 times higher integrated luminosity (**3000-4000fb⁻¹**) in 10 years.
 - Center of Mass Energy will be 14TeV
 - Instantaneous luminosity after leveling is **~5x10³⁴cm⁻²s⁻¹**
 - **Requirement : No major degradation of performance upto 7.5x10³⁴cm⁻²s⁻¹ instantaneous luminosity with 200 multiple interaction per bunch crossing.**

Physics motivation

- Why we need $300 \rightarrow 3000 \text{fb}^{-1}$?

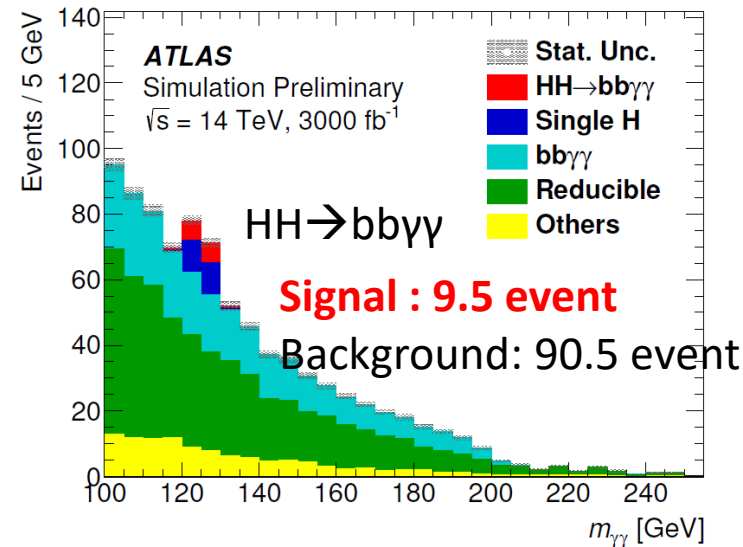
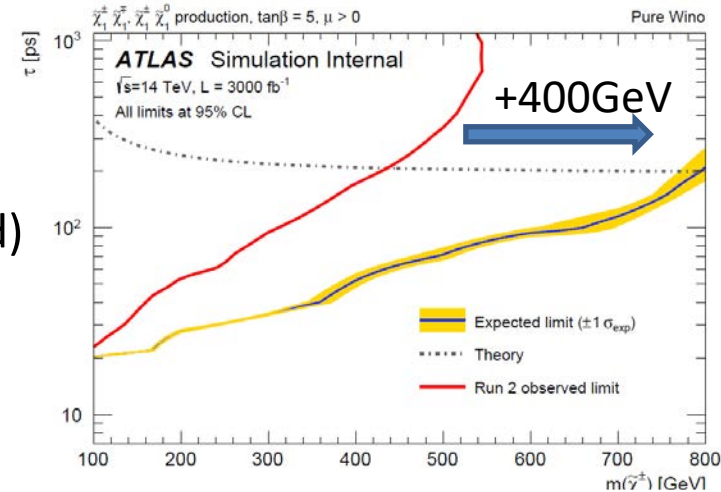
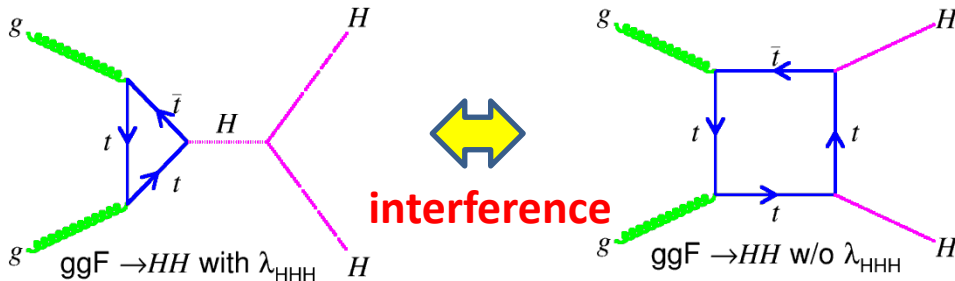
- New Physics

- Especially for the BSM by Weak interaction
- Mass degenerated DM candidate (Long Lived)
 - ex. $\Delta m = 160 \text{ MeV}$ Pure Wino
 - 95% C.L. lower limit $400 \text{ GeV} \rightarrow 800 \text{ GeV}$
 - # of expected signal @ 800 GeV : **11.9 event**

- Higgs measurement

- Precise measurement of Higgs couplings
- Observation of rare decay ($H \rightarrow \mu\mu$)
- **Higgs tri-linear coupling (self-coupling)**

Observe Higgs pair production :

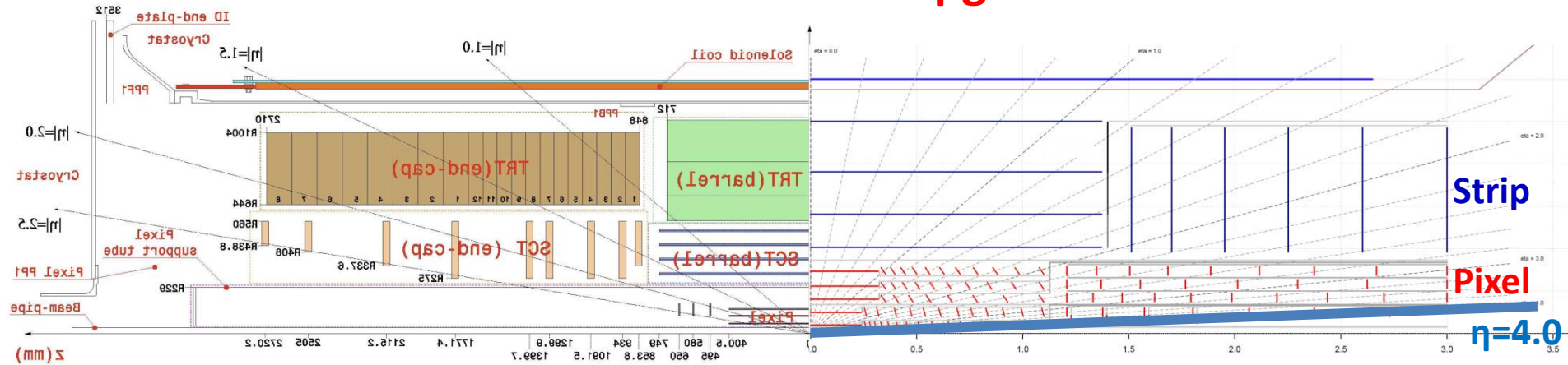


HL-LHC is the only experiment we see these physics in next 15 years

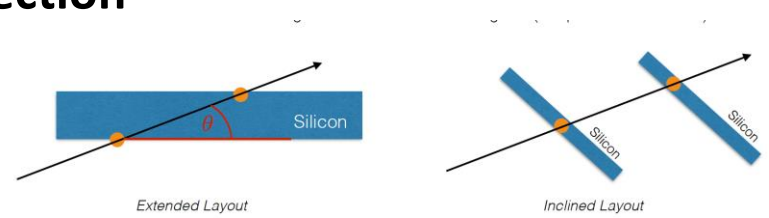
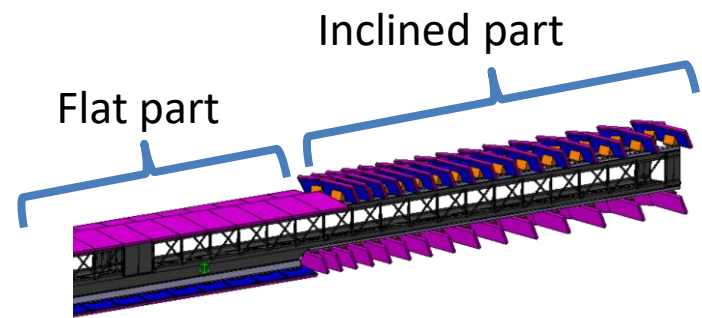
ATLAS inner tracker(ITK) project for HL-LHC

Current ATLAS Detector

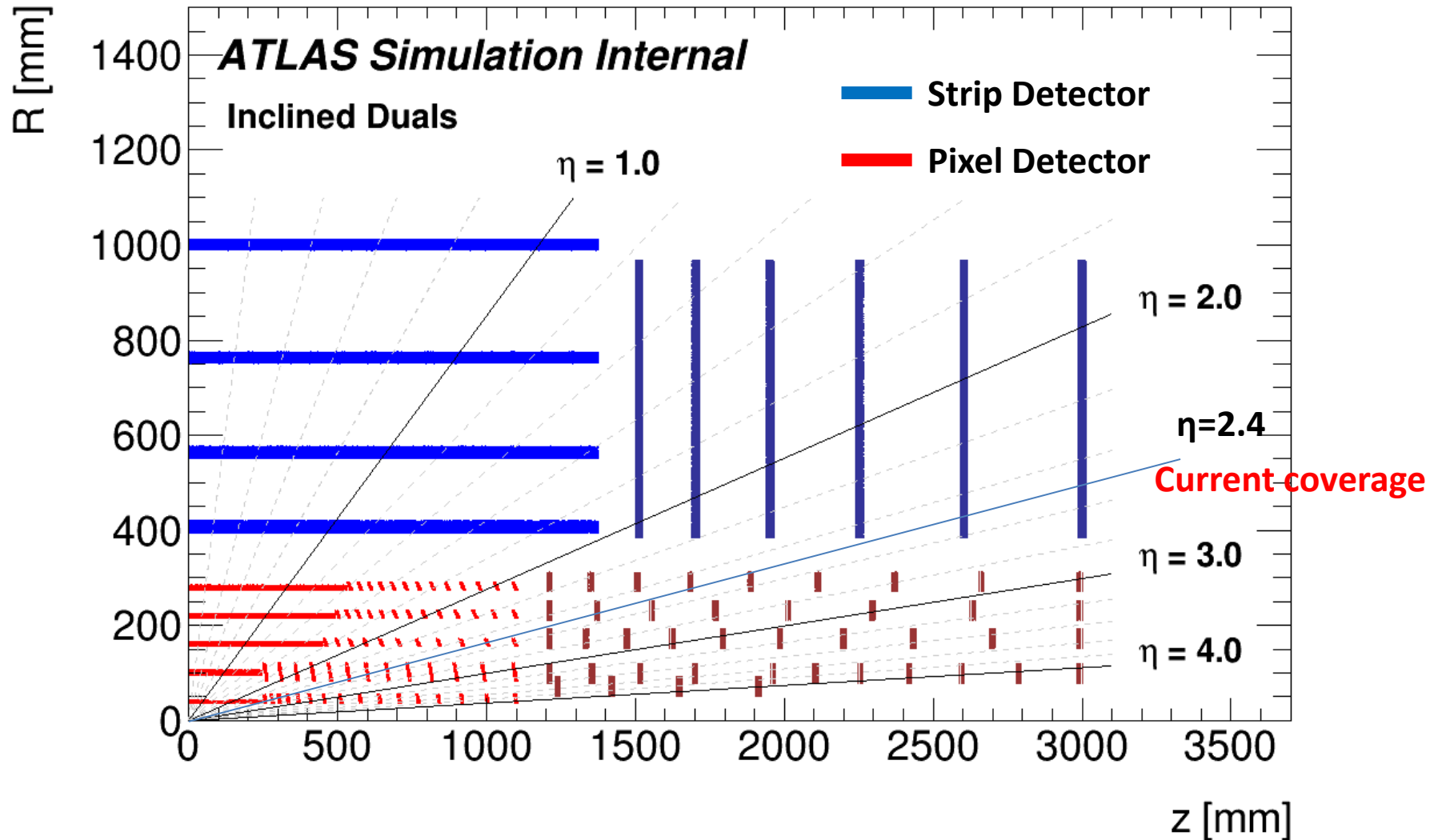
ITK upgrade detector



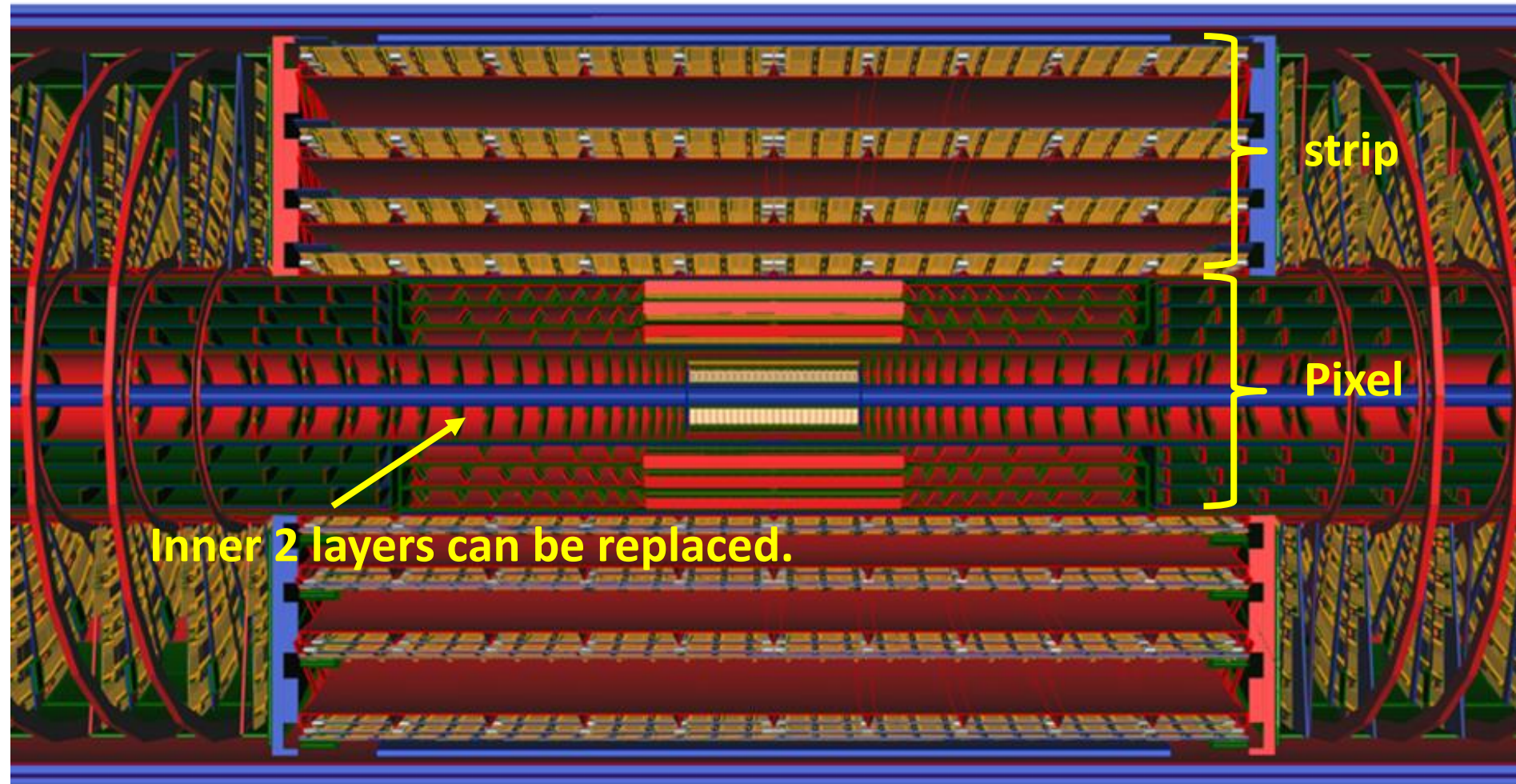
- Larger coverage area
 - Pixel : current 2.7m² → **upgrade 8.2m²**
 - Strip : current 34m² → **upgrade 165m²**
- Higher Forward coverage
 - Current $\eta < 2.5$ → **upgrade $\eta < 4.0$**
 - **Better Pileup removal & background rejection**
- Mechanics : inclined
 - Reduce material
 - Higher tracking resolution.



Inner Tracker (ITk) Layout

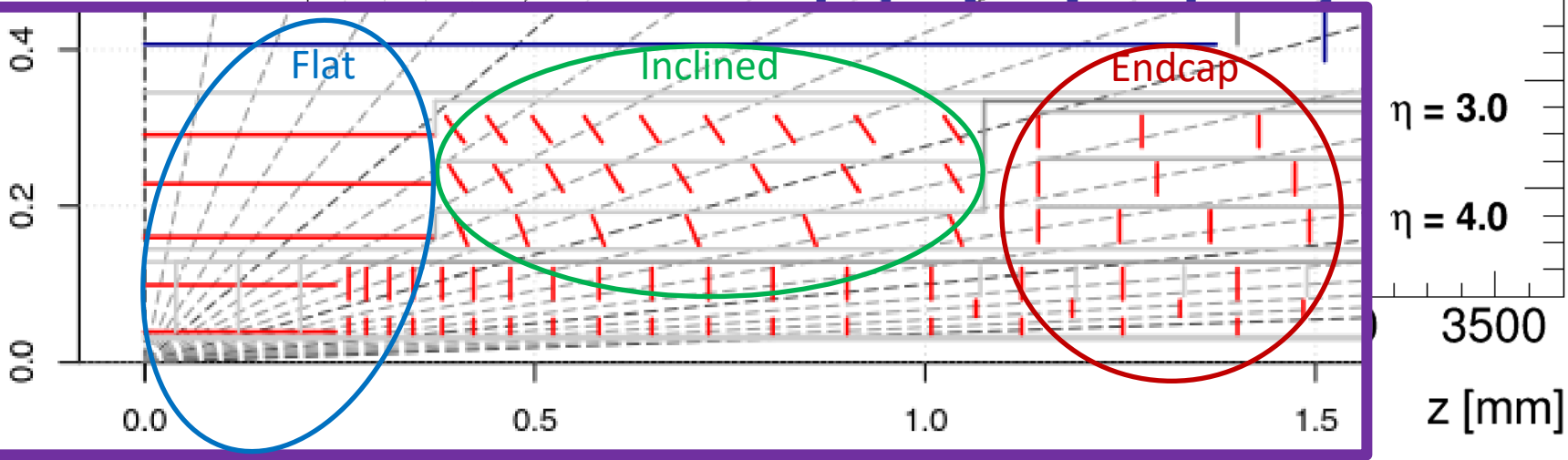
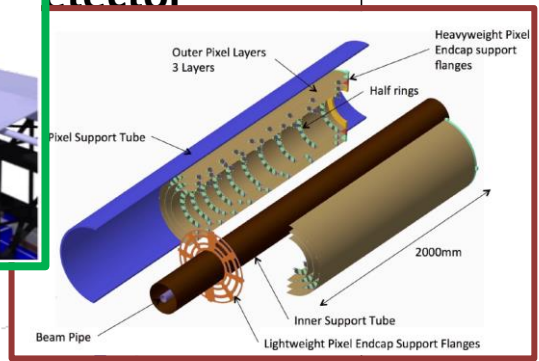
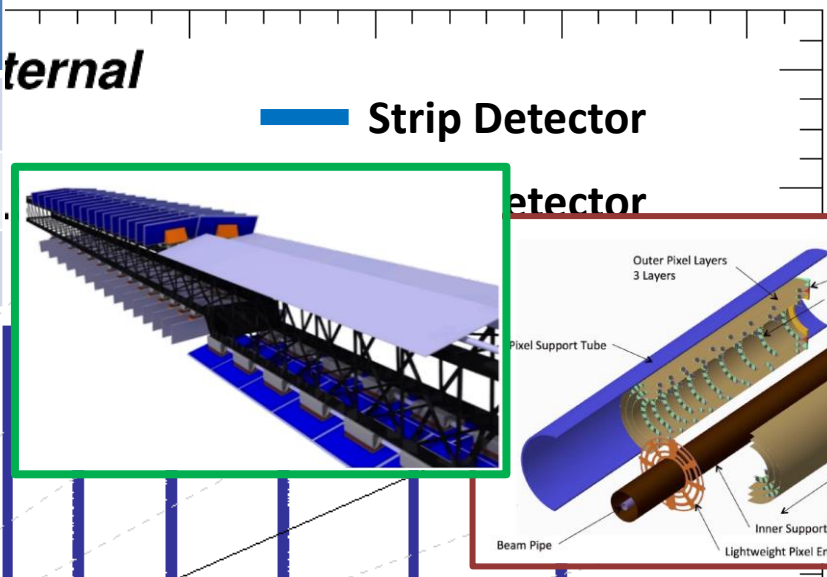
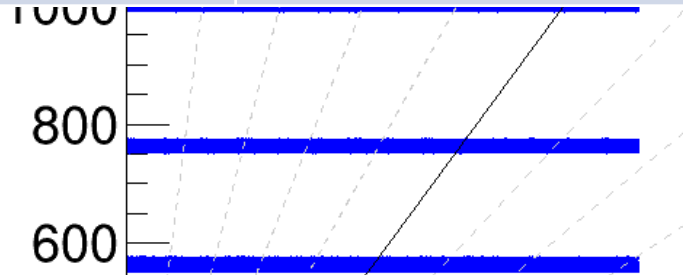


Inner Tracker (ITk) Layout



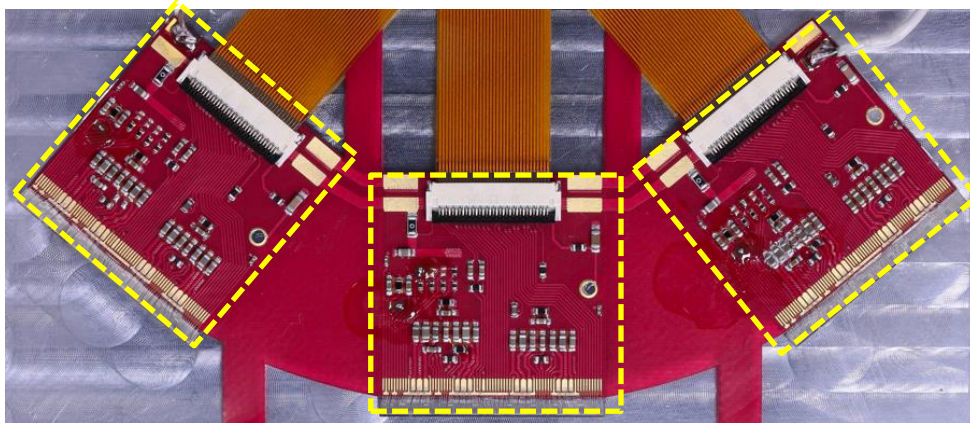
Inner Tracker (ITk) Layout

	Type of sensors
Layer 0	3D type
Layer 1	Thin planar(100um)
Layer 2-4	Thick planar(150um)

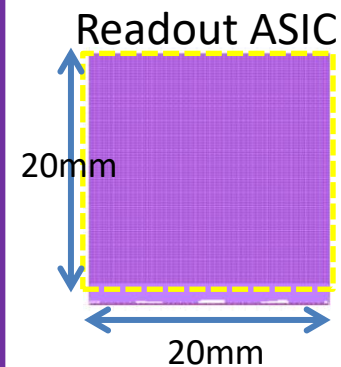
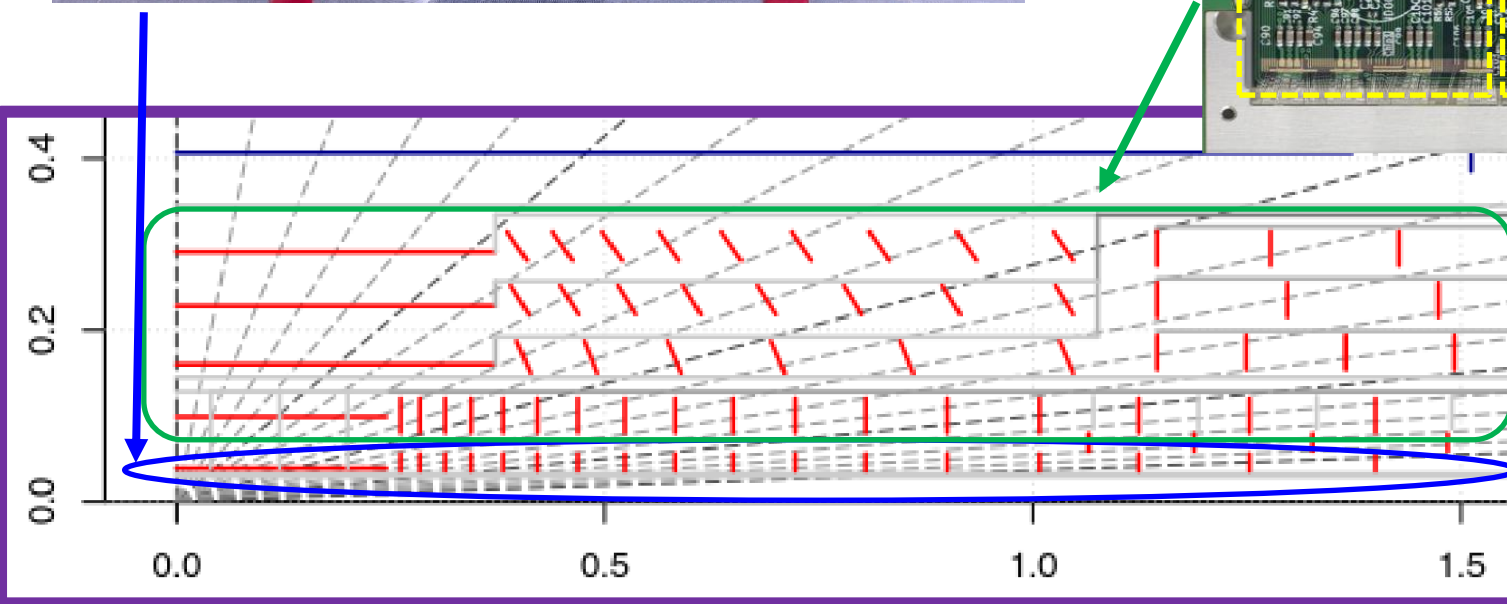
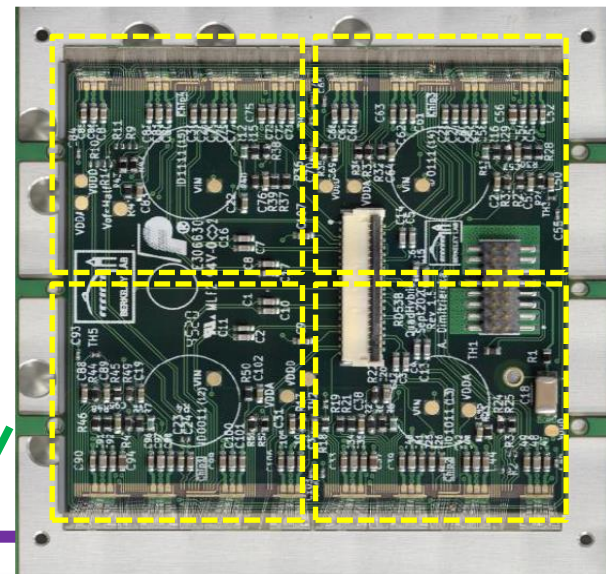


Inner Tracker (ITk) Layout

3D : Triplet structured by single modules

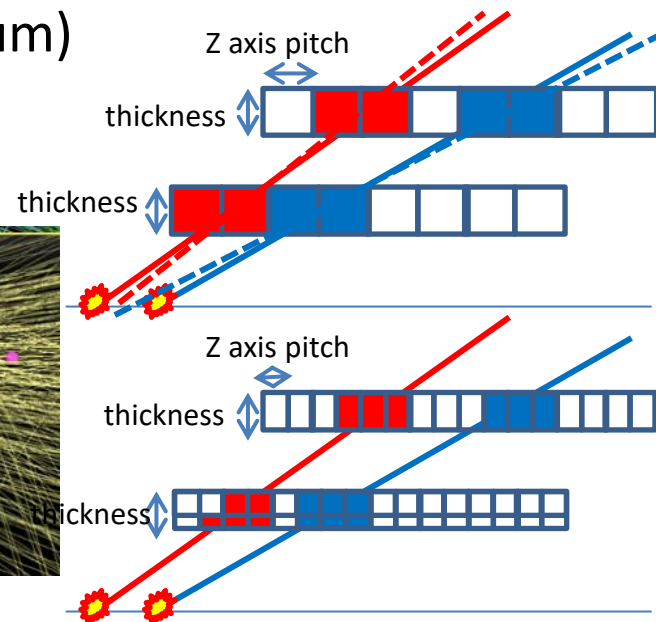
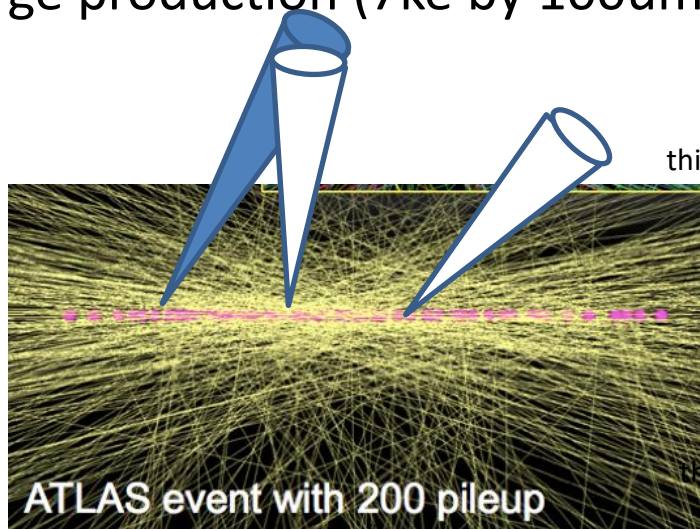
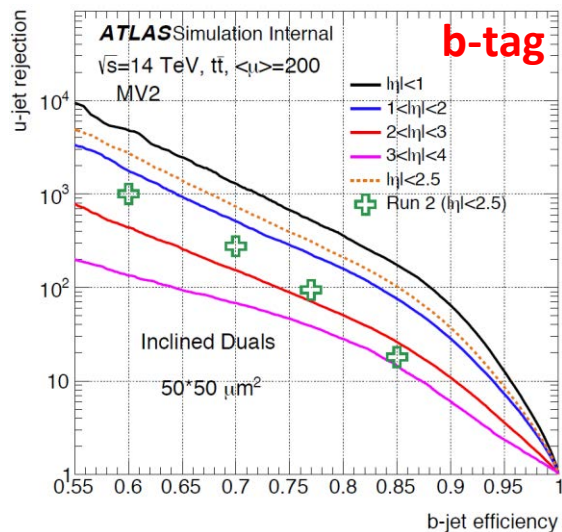
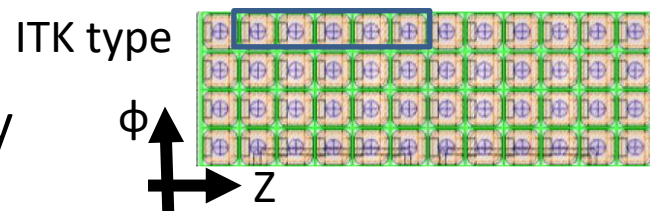
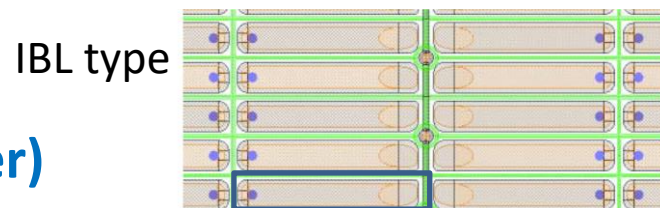


Planar : Quad module (single sensor)



Requirement : Pixel Detector

- Pixel size
 - 1/5 (Z axis) of current pixel (IBL)
 - **50 μm x 50 μm (25 μm x 100 μm inner most layer)**
 - Limitation by readout electronics
- Sensor Thickness
 - Thinner : Material budget + lower occupancy
 - **Layer 0,1 : 100 μm Layer 2,3,4 : 150 μm**
 - Limitation by charge production (7ke by 100 μm)



Requirement : Radiation tolerance

- Expected radiation level @ 4000fb⁻¹

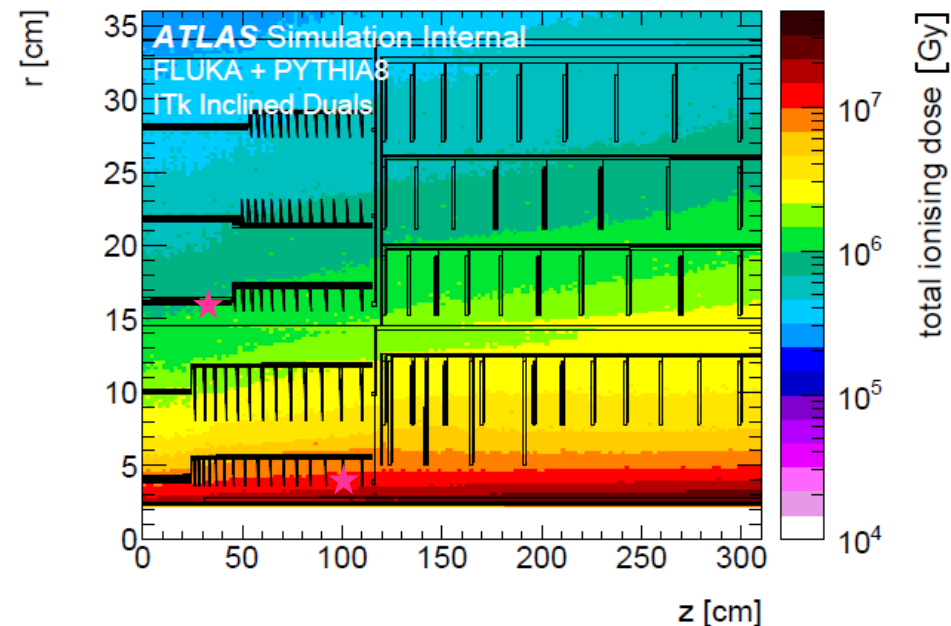
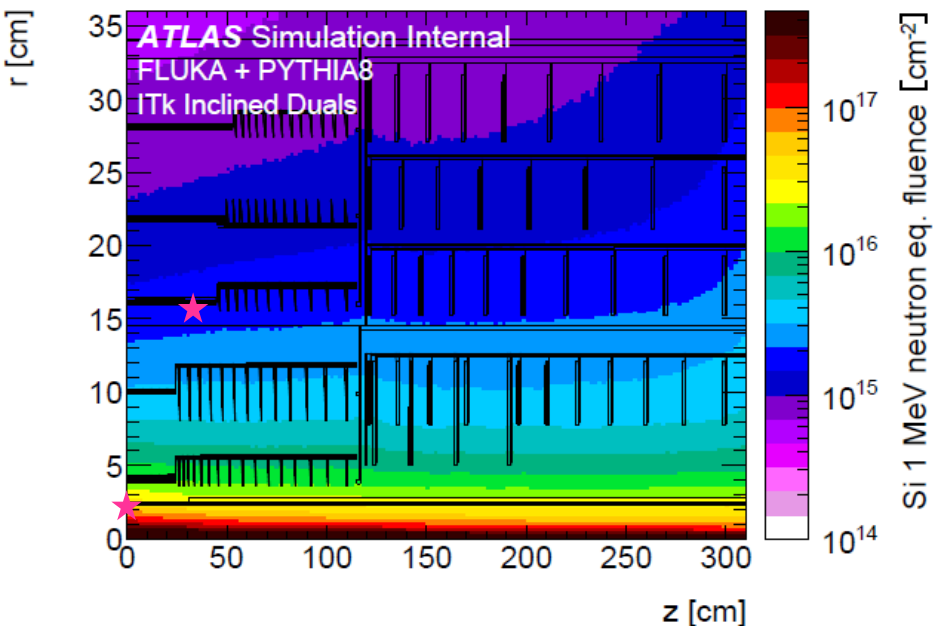
- Non Ionizing Energy Loss :

- L2 2.8x10¹⁵ neq /cm² L0 2.6x10¹⁶neq/cm²

- Total Ionizing Dose :

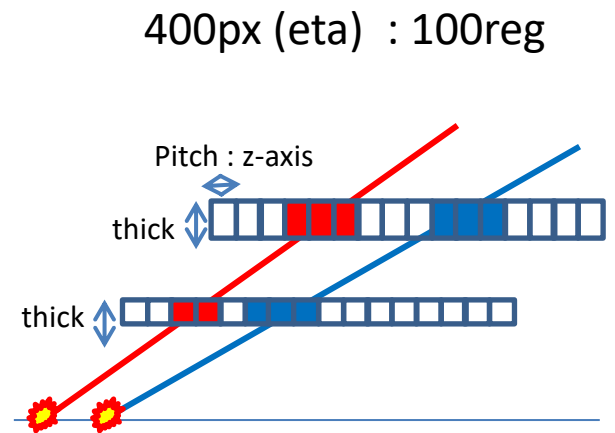
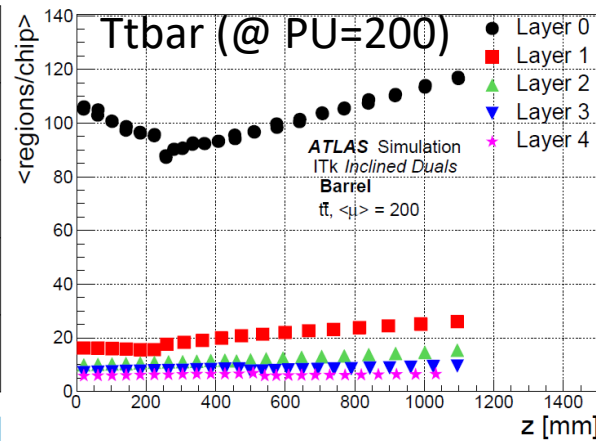
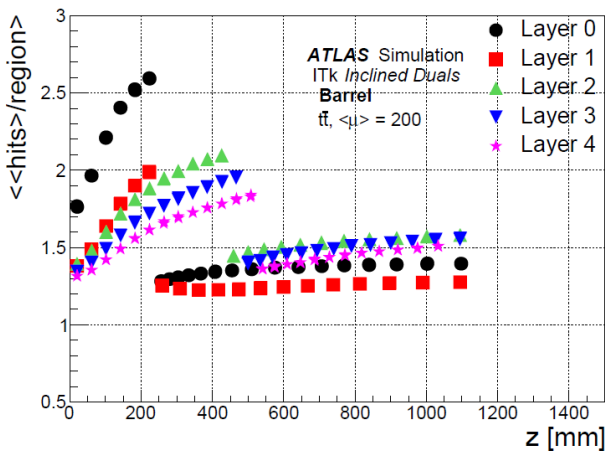
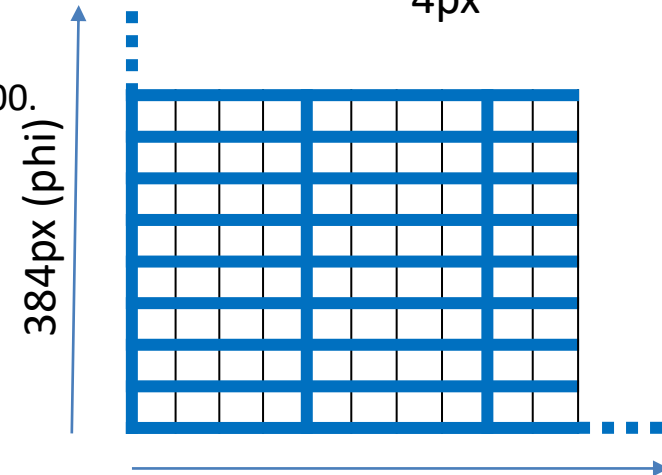
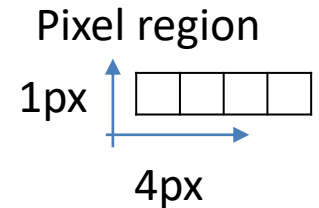
- L2 1.6MGy L0 19.8MGy

L0, 1 can be replaced
@ 2000fb-1



Requirement : Front-End ASIC

- **ASIC size** : 20mmx20mm → limited by ASIC fabrication process (Yield)
 - **Pixel size** : 50umx50um → limited by the size of threshold DAC (5bit).
 - **TSMC 65nm fabrication process.**
 - Data rate / 20mmx20mm (400x384px)
 - **4 bit** Time-over-Threshold (**ToT**) based ADC.
 - Equivalent Noise Count(**ENC**) ~**50e**, minimum in-time threshold 600.
 - Define **Pixel region** with 1x4 pixel and readout together.
 - Readout 32bit / region
 - 16 bit (7bit+9bit) address + 4 x 4 bit ToT (Less data >1.6hit/region.)
 - Data Rate = reg-hit/chip * Nbit * f_{trig} * N_{chip}
 - Layer0 : 100 * 32bit * 1MHz ~ **3.2Gbps**
 - Layer3 : 5 * 32bit * 1MHz * 4(quad) ~ **0.6Gbps**
- **1.28Gbps x 4 lane readout** (4 lane for L0 but less lane for outer)



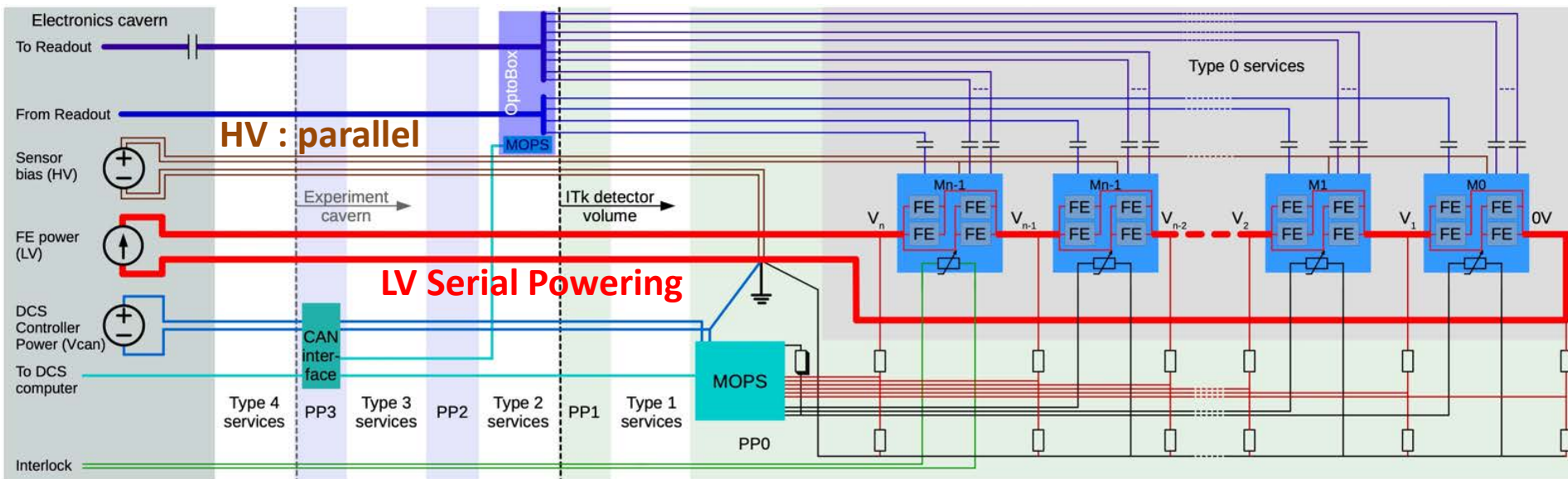
Power dissipation / consumption

- Power dissipation
 - Sensor power : $< 50\text{mW}/\text{cm}^2$
 - After radiation damage : $45\mu\text{A}/\text{cm}^2 @ 600\text{V} @ -25^\circ\text{C}$
 - FE ASIC $< 0.7\text{W}/\text{cm}^2$ (12W / 4chip module)**
 - Requirement from cooling power
- Current consumption
 - Quad chip module : $< 6\text{A} \rightarrow 1.5\text{A}/\text{chip}$
 - Requirement from Power supply
 - $1.8\text{V} \cdot 1.5\text{A} / 4\text{cm}^2 = 0.67\text{W}/\text{cm}^2$
- Powering scheme:

Leakage current after radiation damage

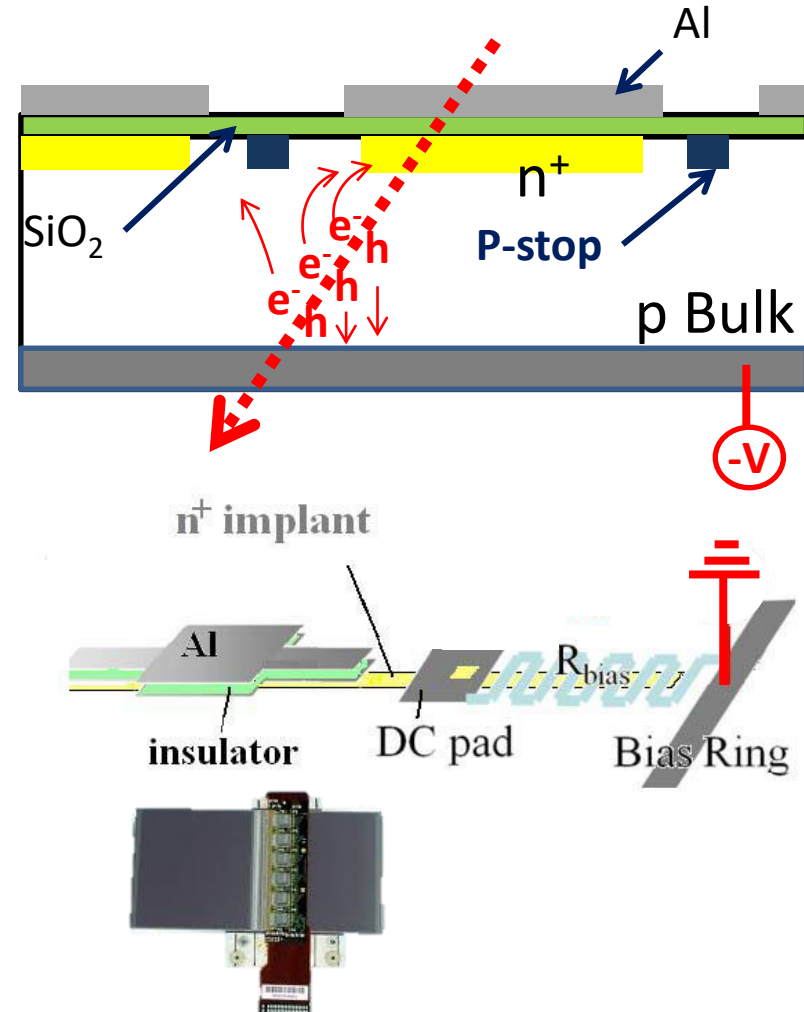
	$\Phi = 2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$	$\Phi = 5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
Total leakage current	$< 25 \mu\text{A}/\text{cm}^2 @ 400\text{V}$ (Lot-1) $< 20 \mu\text{A}/\text{cm}^2 @ 300\text{V}$ (Lot-2)	$< 45 \mu\text{A}/\text{cm}^2 @ 600\text{V}$ (Lot-1) $< 35 \mu\text{A}/\text{cm}^2 @ 400\text{V}$ (Lot-2)
Breakdown voltage	$> 400 \text{ V}$ (Lot-1) $> 300 \text{ V}$ (Lot-2)	$> 600 \text{ V}$ (Lot-1) $> 400 \text{ V}$ (Lot-2)
Hit efficiency at orthogonal incidence	$> 97.0\%$ at 400 V (Lot-1) $> 97.0\%$ at 300 V (Lot-2)	$> 97.0\%$ at 600 V (Lot-1) $> 97.0\%$ at 400 V (Lot-2)

*Lot1 150um Lot2 100um



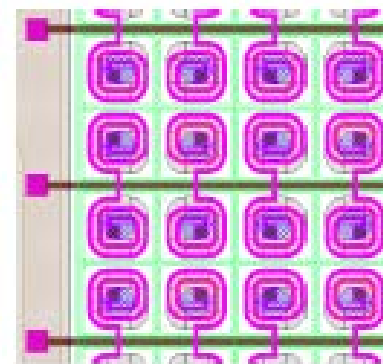
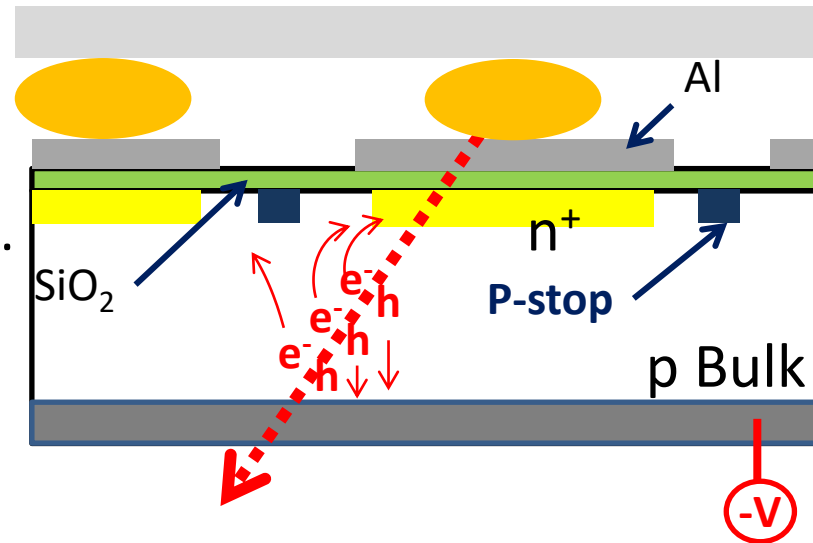
Semiconductor tracking detector

- Basic principle :
 - Backside is negative bias and n+ is ground.
 - Detect electron-hole pairs created by ionizing energy loss from MIP particle.
- Strip detector
 - n+ can easily ground at the end of strip.
 - Readout usually via “wire bonding” strips to the readout ASIC.



Semiconductor tracking detector

- Basic principle :
 - Backside is negative bias and n+ is ground.
 - Detect electron-hole pairs created by ionizing energy loss from MIP particle.
- Strip detector
 - **n+ can easily ground at the end of strip.**
 - Readout usually via “**wire bonding**” strips to the readout ASIC.
- Pixel detector (new technology)
 - **Electrode placed two dimensionally.**
 - To ground all pixels, high resistivity biasing grid is necessary.
 - Readout ASIC is connected by “**bump-bonding**”.

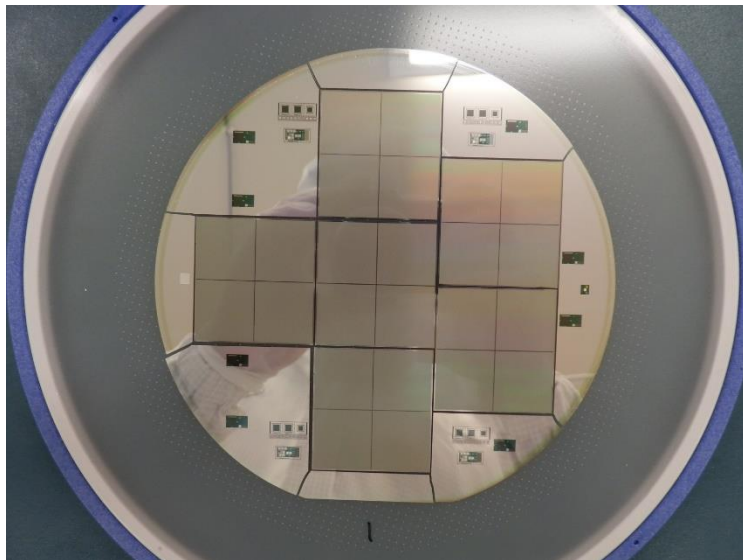


Our development is together with Hamamatsu Photonics K.K (HPK)

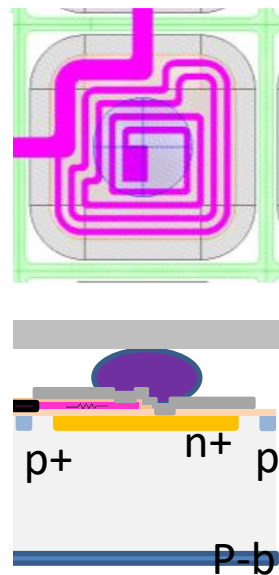
Final Sensor design

- Basic Sensor structure has been developed during R&D
- Final pitch (50umx50um) pixel size and full size (40mmx40mm) sensors are produced.
- Full size sensor and ASIC are produced in 2019.
 - **Now sensor pre-production is ongoing with final design.**
 - **Quality control and Quality Assurance are prepared.**

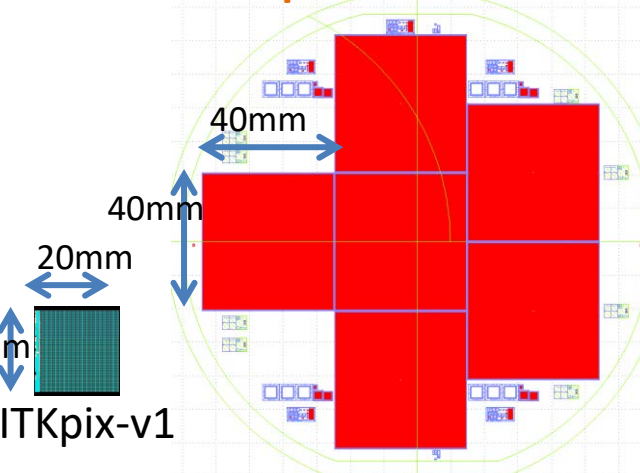
40mm x 40mm full size prototype sensors



40mm x 40mm production modules (20mm x 20mm ASIC size)



HPK Pre-production mask



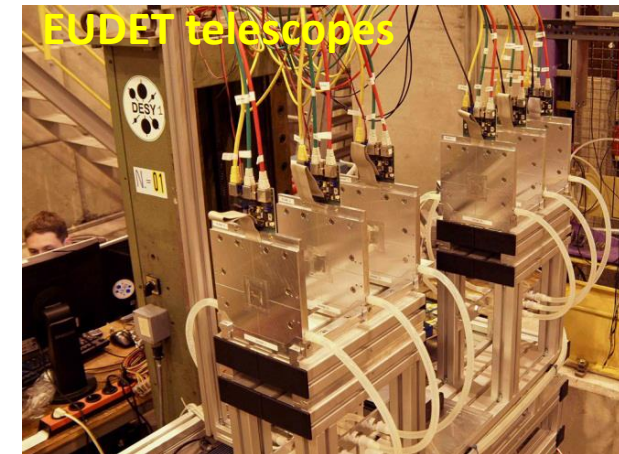
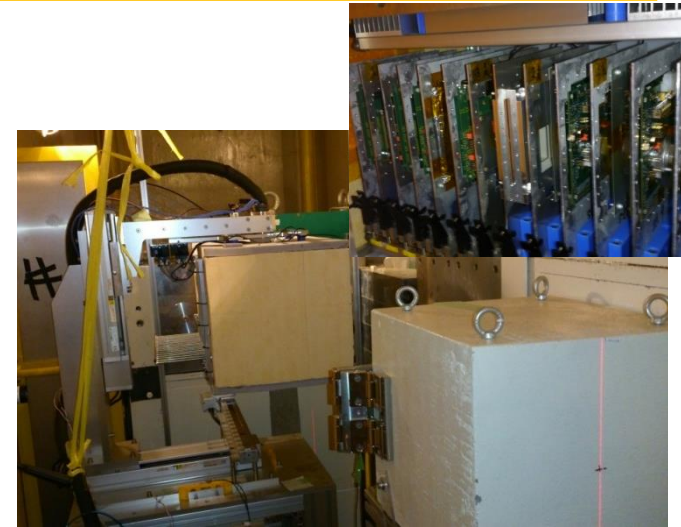
Irradiation and Testbeam

- CYRIC@Tohoku Univ.

- An irradiation facility with **70MeV proton beam** (**$\sim 1\mu\text{A}$ beam current**).
 - 3-5 hours for $3 \times 10^{15} n_{\text{eq}}/\text{cm}^2$ irradiation with (600nA beam)
- This allows 2-3 pixel modules with Al plate at the same time (3% E loss/module).
- Operated at **-15°C temprature** with dry N_2 gas.
- Scanning over full pixel surface at irradiation.

- **Testbeam**

- **Extremely important to test device performance**
- Efficiency/Noise monitoring during production
- Testbeam facility
 - **CERN SPS : 120GeV π^+ beam**
 - DESY : 4-5GeV e^+ beam
 - FNAL : 120GeV proton beam
- Telescope planes (Track pointing to device)
 - EUDET based on MIMOSA26 monolithic CMOS detector placed in beamline at CERN/DESY/SLAC (**$\sim 3\mu\text{m}$ pointing resolution**).
 - Huge experience of the testbeam operation as having testbeam 3-4 times a year

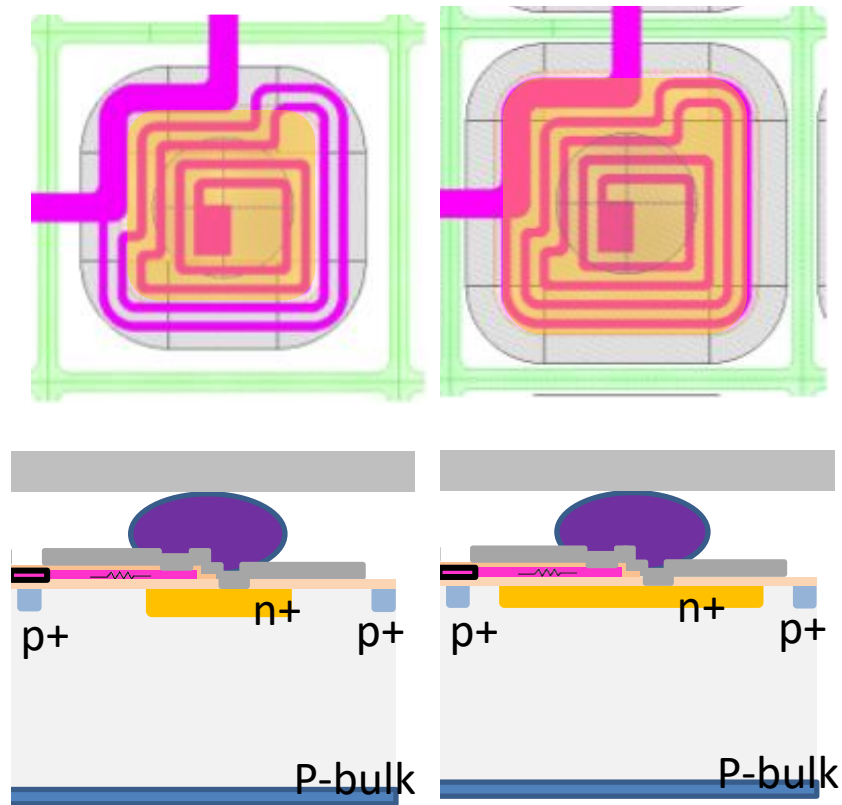
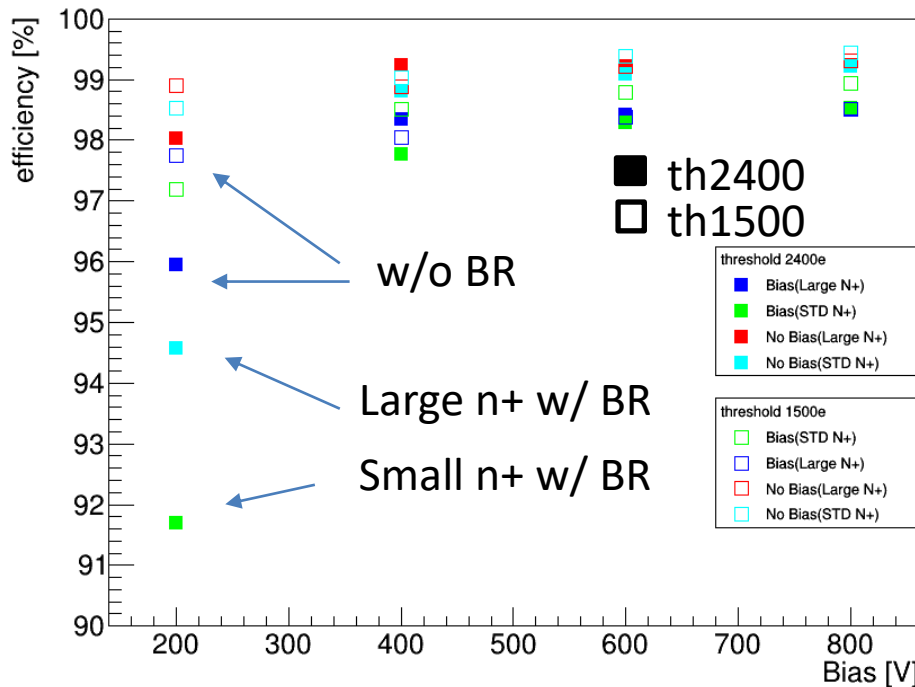


Efficiency result (irrad $3 \times 10^{15} n_{eq}/cm^2$)

- Efficiencies of HV scan 200-800V have been evaluated.
 - Analyzed both 1500e and 2400e threshold data for different types.
 - **All types have over 98% efficiency at 600V.**
 - 1500e threshold results have over 99% efficiency.
 - Small n+ w/ BR have low efficiency at 200V

K. Nakamura Pixel 2018

KEK53-5 Efficiency



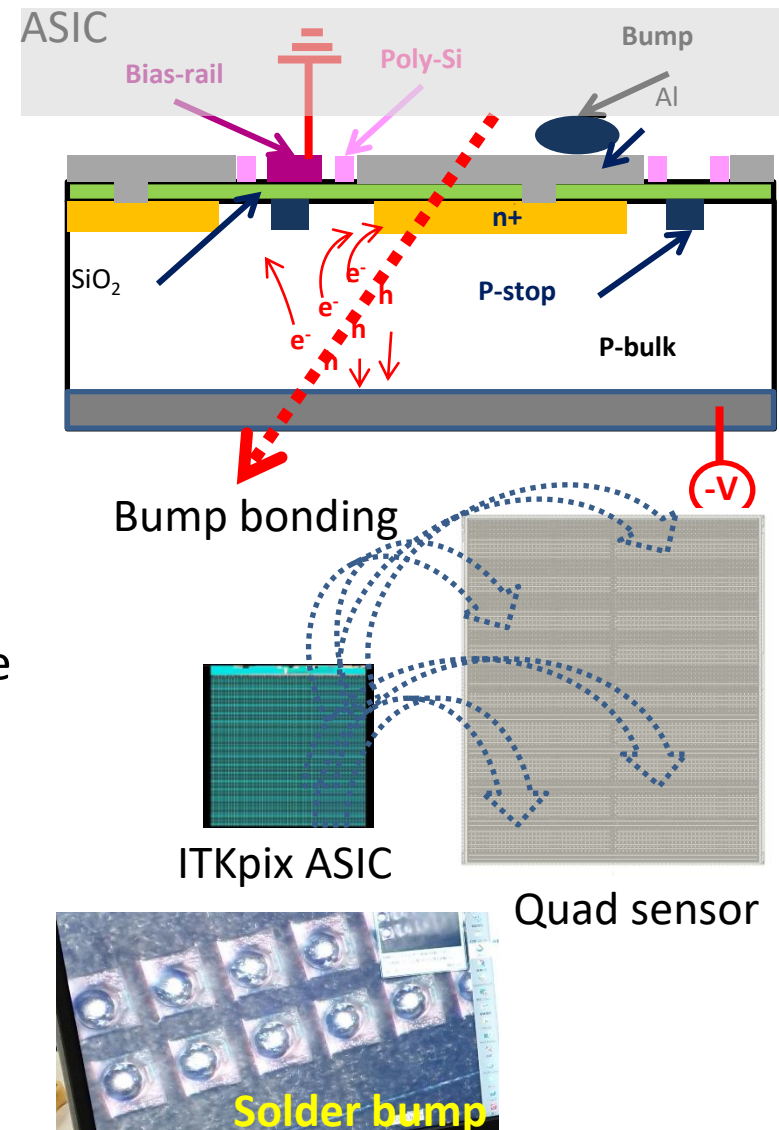
Sensor – ASIC attachment at HPK

- To readout signals from 2 dimensionally placed electrodes (pixels), readout ASIC needed to be connected.

- the signal from each channel is read out through a solder bump

- **Bump bonding** :

- Solder bump deposition to the ASIC side
- Under bump metallization to Sensor side
- Flip-chipping : 4 chips to one sensor.



Sensor – AISC attachment at HPK

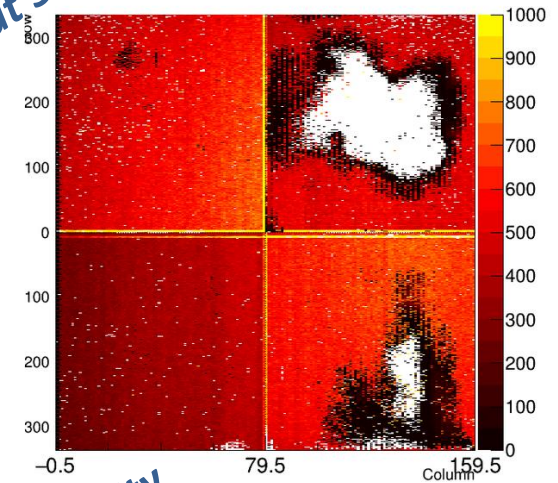
Development of Lead-free(SnAg) Bumpbonding (Since 2012)

- 1. No Flux used (to avoid corrosion)**
 - confirmed flux improve connection, though
- 2. No backside compensation**
 - Improvement of Vacuum chuck jig to hold and flatten the ASIC/Sensor...(jig size ~ FE-I4 area)
- 3. Special UBM (key element: confidential...)**
 - Simple Ni/Au UBM do not reach 100% yield ...
- 4. Hydrogen plasma reflow** to remove surface oxide

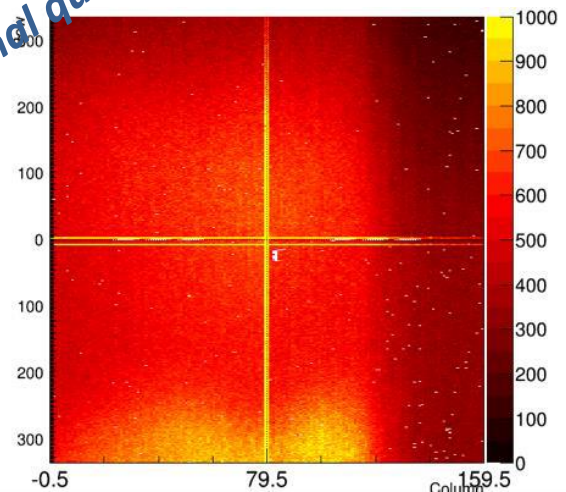
Thin sensor/Thin ASIC : 150um/150um

- **Established Bumpbonding method in the beginning of 2016.**
- Quite stable quality for both single and four ASICs. 100% yield for last one year (>100 chips are bumpbonded.)

Without 3 and 4



Final quality

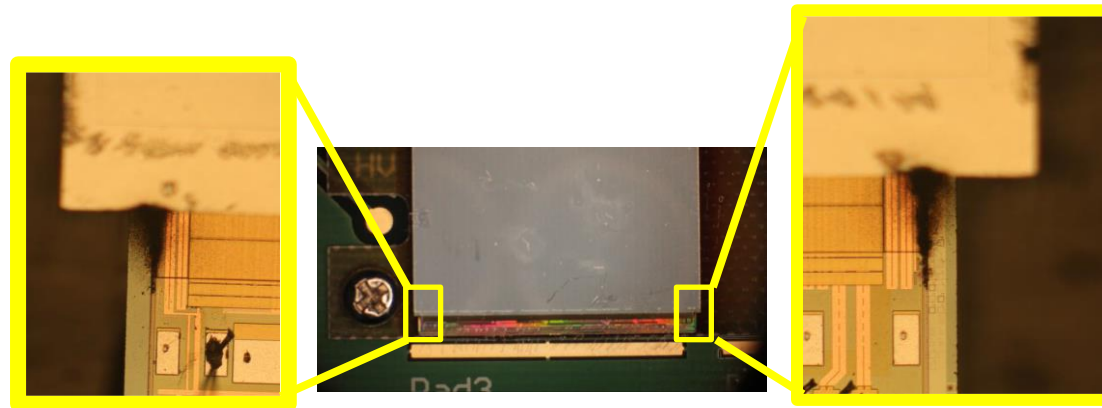
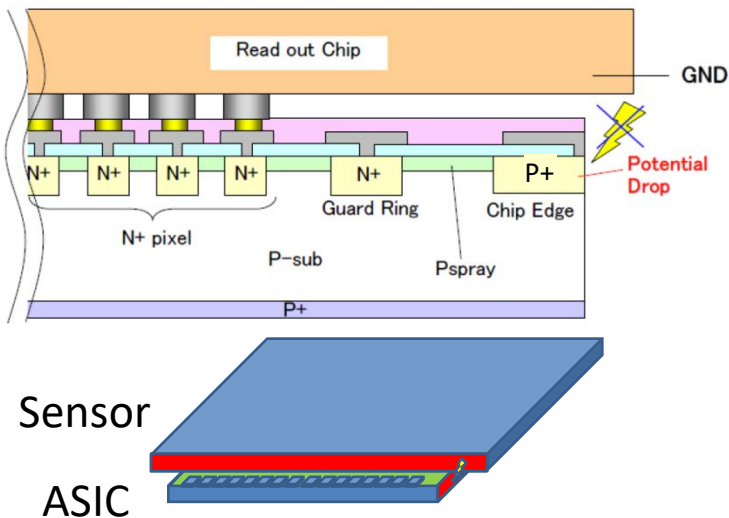
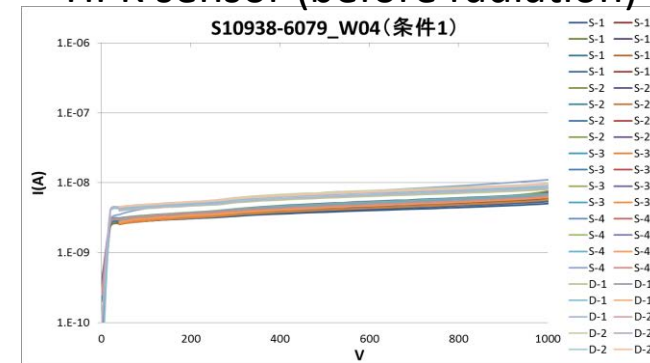


End of life and HV spark protection

- In principle, it's break down voltage.
 - **HPK sensors are very good quality ($V_{bd} > 1000V$)**
 - Other vendor : $V_{bd} \sim \text{Full Depletion}(V_{fd}) + 70V$.
 - V_{fd} voltage go up by radiation damage
 - End-of-life when $V_{bd} < V_{fd}$
- HV spark protection
 - **Large potential difference btw ASIC-Sensor. Spark happened $\sim 400V$.**
 - HV protection is necessary.
 - **Parylene coating** : survive upto 1000V

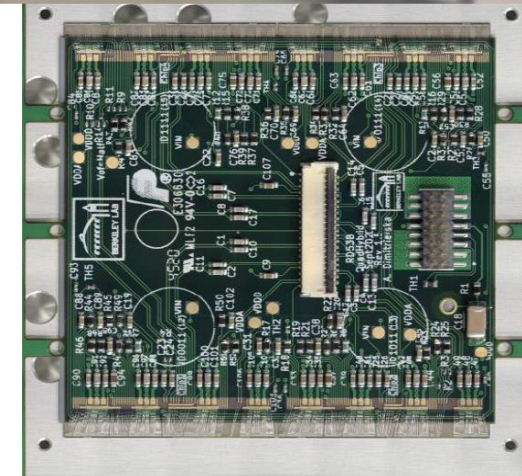
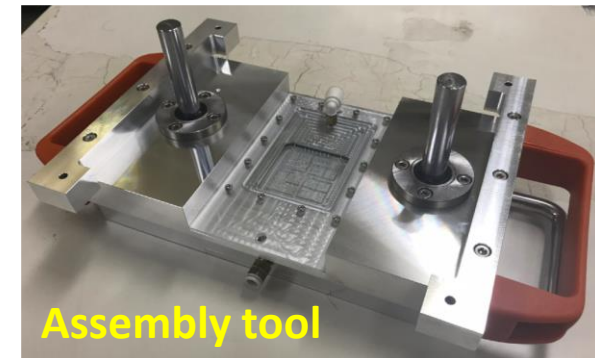
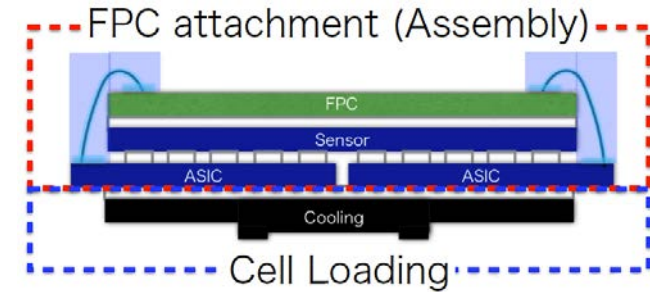
(Dicing and backside process)

HPK sensor (before radiation)



Flex assembly and CTE mismatch

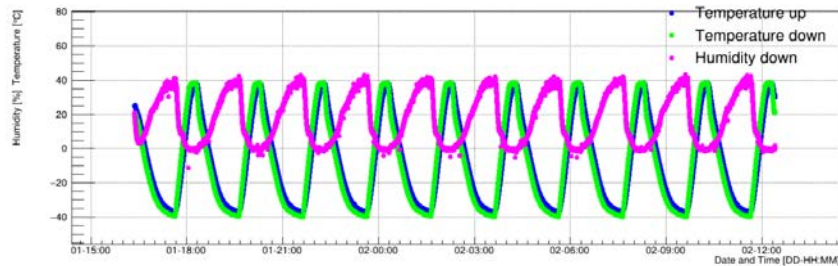
- To read signal from ASIC, Flex Printed Circuit (FPC) is glued to the module by Araldite 2011.
- Cooling TPG/CFRP will attach to the backside of ASIC.
- Then wire bond ASIC pad to FPC.
- Coefficient of Thermal Expansion (CTE) is different for silicon/copper/Carbon.
 - E.g. Silicon 2.6ppm/°C Copper 16.7ppm/°C
- Huge bump stress during thermal cycling.
 - **During 10 years operation, expected 400 times TC from -45°C to 40°C**
 - Qualification : 100 cycle with -55°C to 60°C Temp range



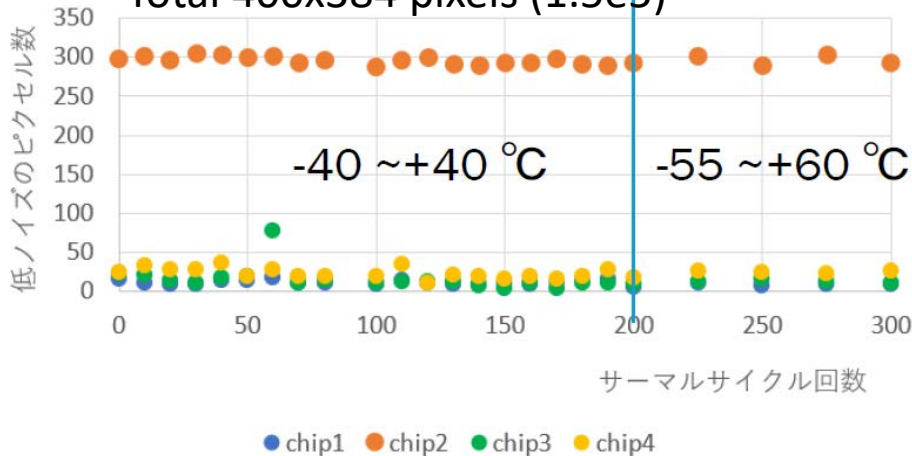
Flex assembly and CTE mismatch

- The close-to-final condition of modules
 - No bump delamination increased during thermal cycle.

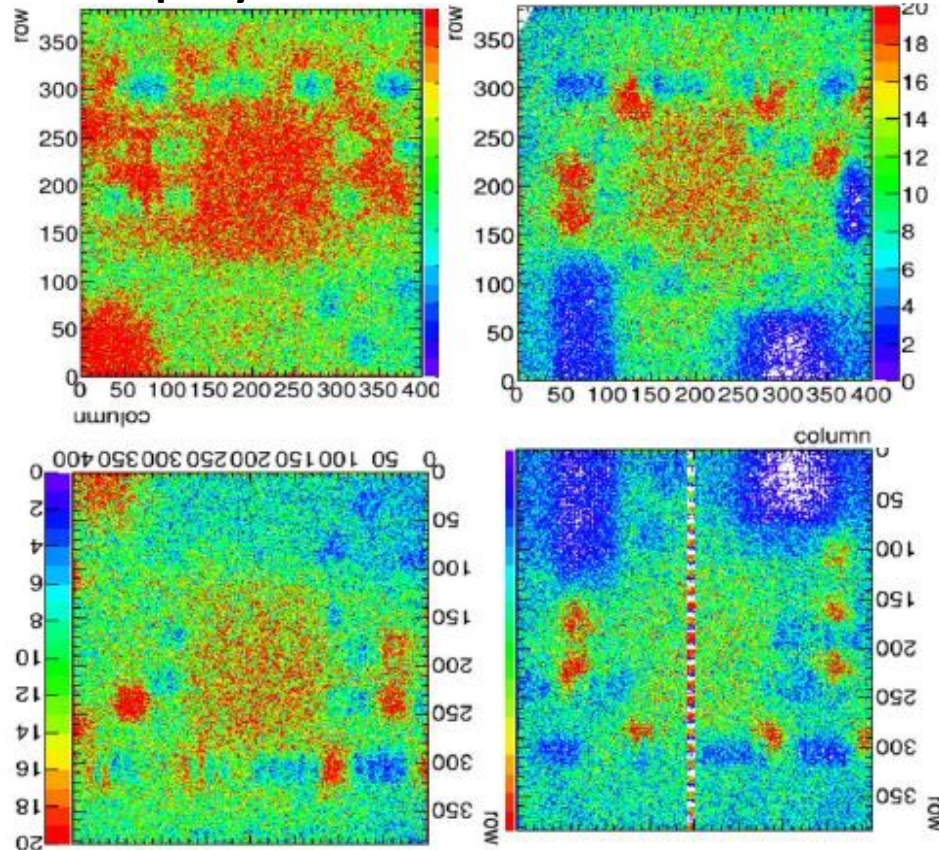
Temperature cycle in climate chamber



Total 400x384 pixels (1.5e5)



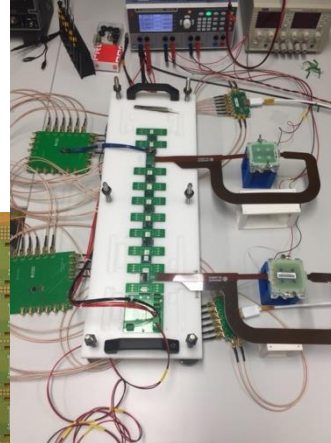
^{90}Sr β ray source results



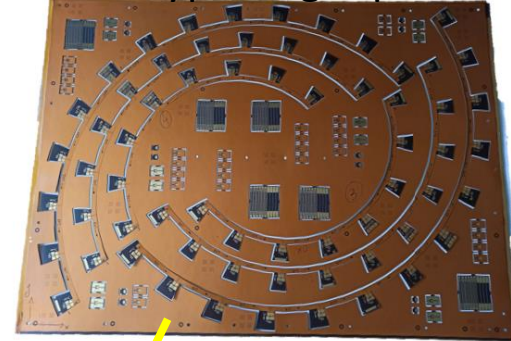
Support & services

- Prototyping

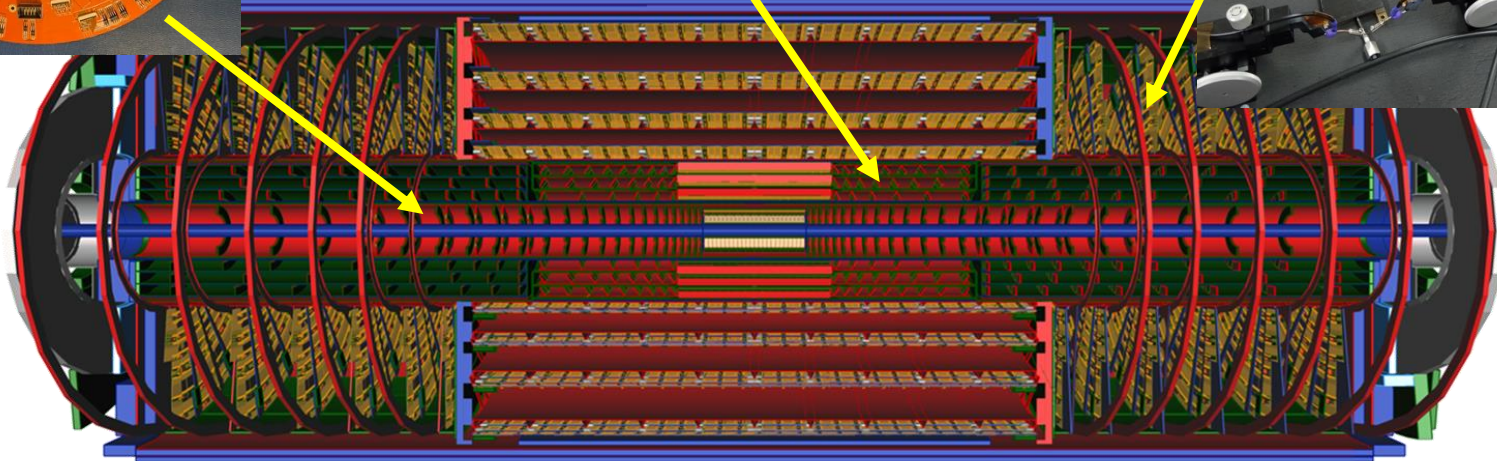
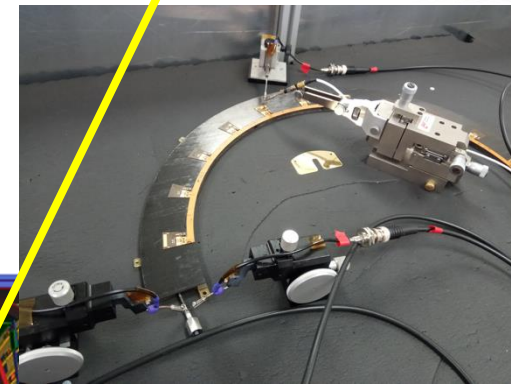
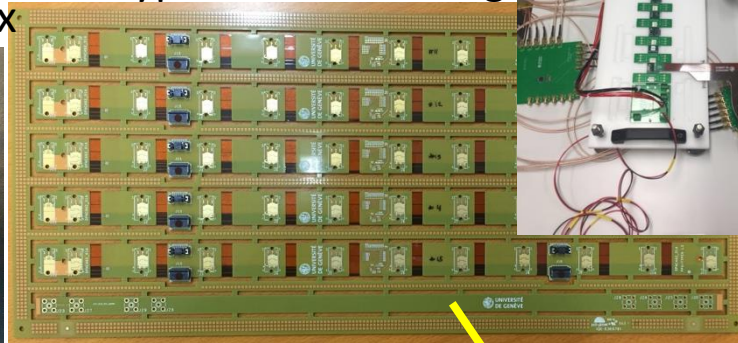
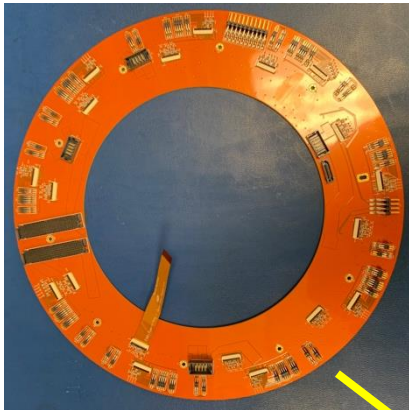
Outer Barrel
Prototype of inclined ring



Prototype ring tape

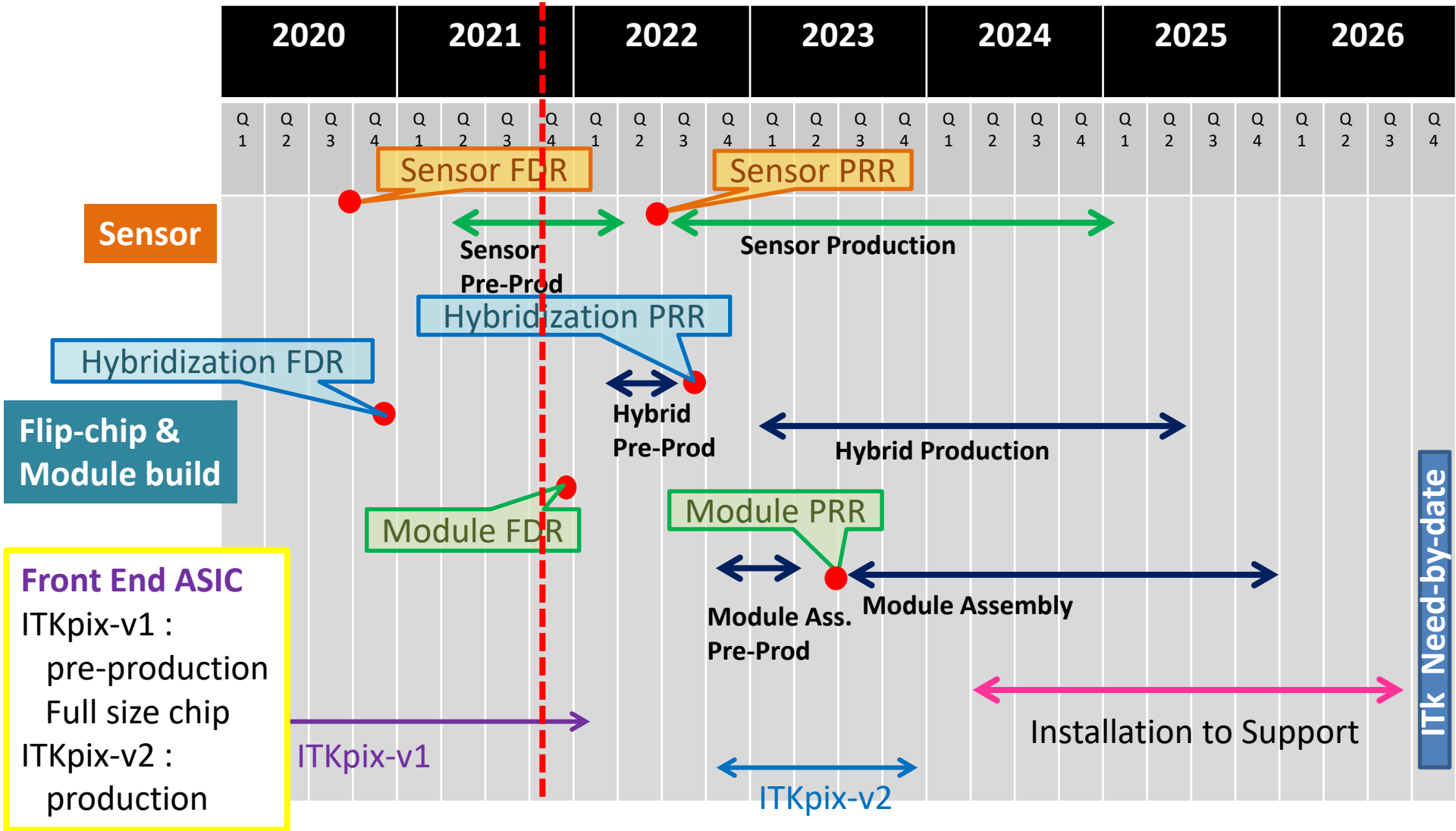


Layer 1 Type-0 ring flex



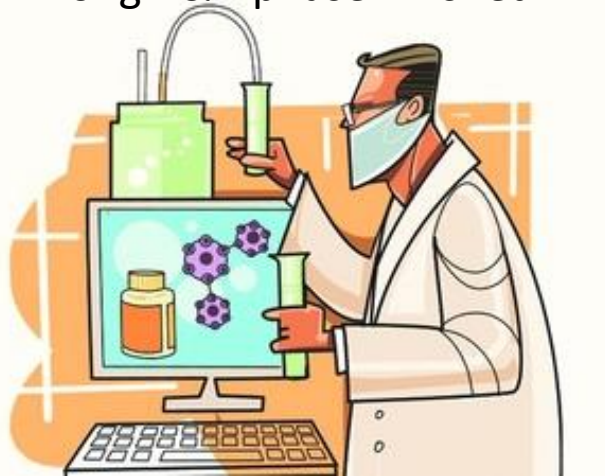
Schedule

PDR : Preliminary Design Review
 FDR : Final Design Review
 PRR : Production Readiness Review



Conclusion

Long R&D phase finished



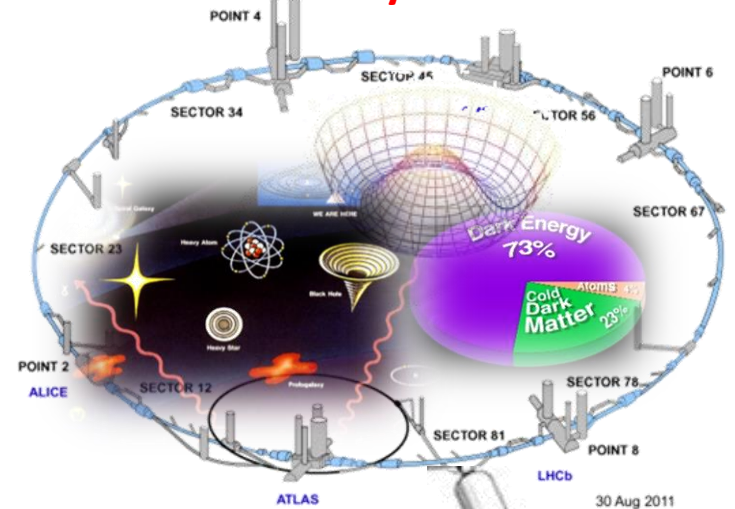
Starting Construction phase:
Pixel sensor pre-production started



Defined **Final Design** now



Will obtain discovery machine in 2027!

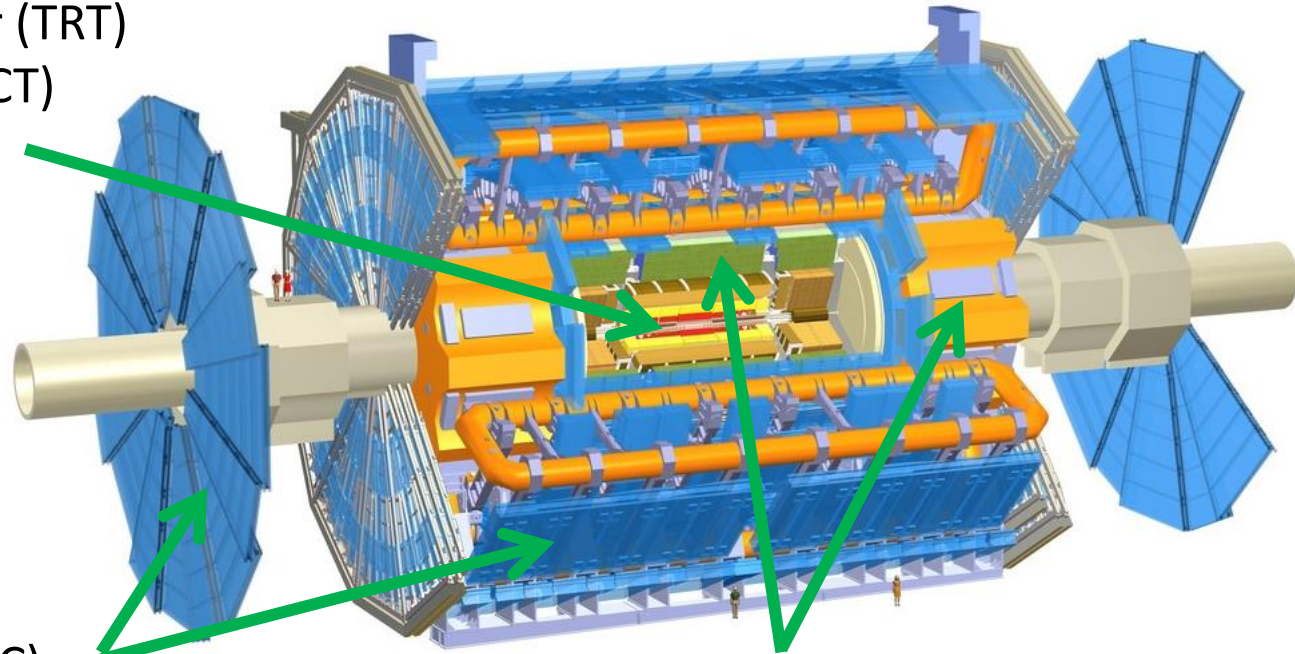


backup

ATLAS Detector Upgrade

Inner Tracking Detectors

- Straw Tube gas chamber (TRT)
- Silicon Strip Detector (SCT)
- Pixe Detector (Pixel)



Muon Detectors

- Trigger chamber (TGC, RPC)
- Drift Tube chamber (MDT)
- [Toroid Magnet]

Calorimeter

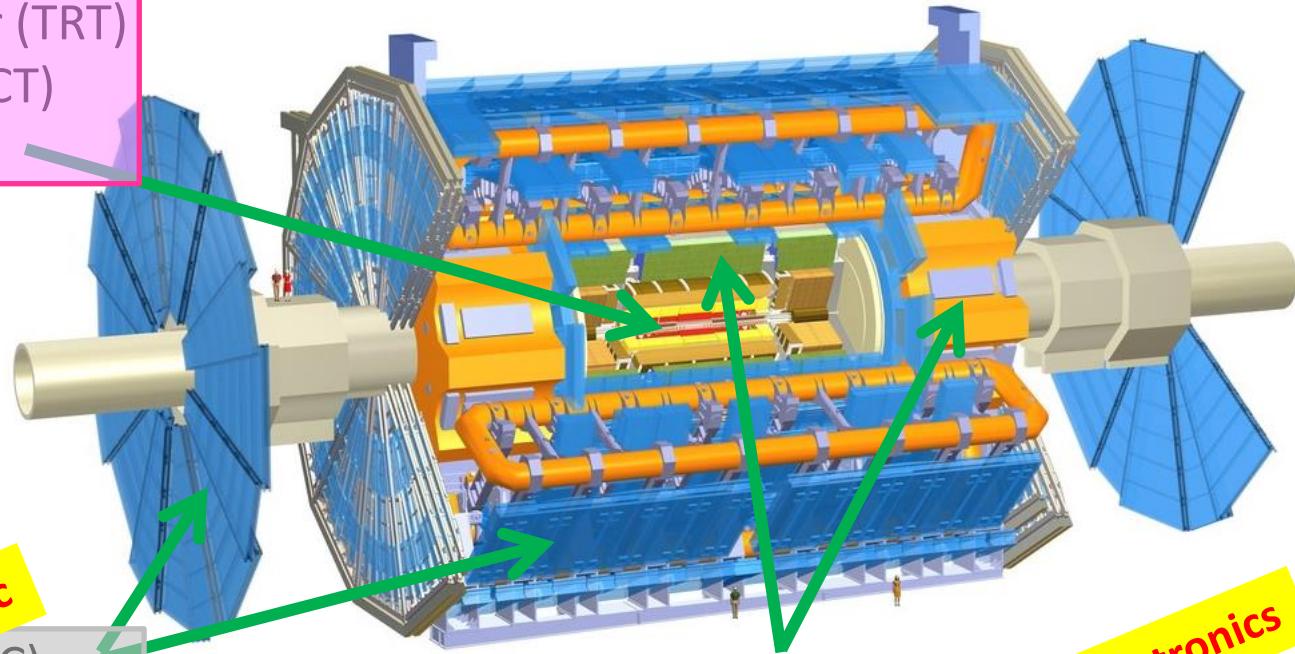
- LAr EM calorimeter
- Hadron calorimeter
- Forward calorimeter
- [Solenoid Magnet]

ATLAS Detector Upgrade

Inner Tracking Detectors

Straw Tube gas chamber (TRT)
Silicon Strip Detector (SCT)
Pixe Detector (Pixel)

Replace All tracking
To all silicon detectors



Muon Detectors

Trigger chamber (C, RPC)
Drift Tube Chamber (MDT)
[Solenoid Magnet]

Improvement of Trigger Logic

More flexible trigger system

Calorimeter

Large Calorimeter
Central calorimeter
Forward calorimeter
[Solenoid Magnet]

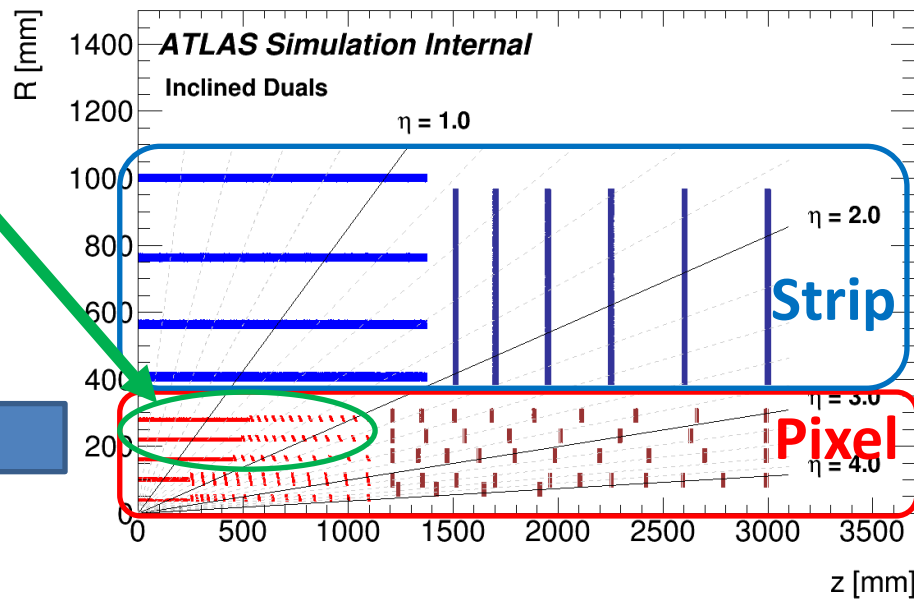
Improvement of Readout Electronics

No detector replacement

ATLAS Pixel Detector Upgrade

- Japan group : Pixel Detector development
 - Target : 3rd – 5th layers
 - High Efficiency Sensor design
 - Readout ASIC and DAQ development
 - Sensor – ASIC attachment
 - Flex PCB design and assembly
 - Module loading to the support

Contributing to all steps
Build detector in Japan



Layer 2 + Layer 3 Demonstrator

