ILC 用衝突点検出器の設計に向けた SOI ピクセル検出器としての取り組み

Activities of SOI Pixel Development for the Design of Vertex Detector at the ILC

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原和彦，鈴木尚紀，大森匠（筑波大）

武田彩希，三住京也（宮崎大）

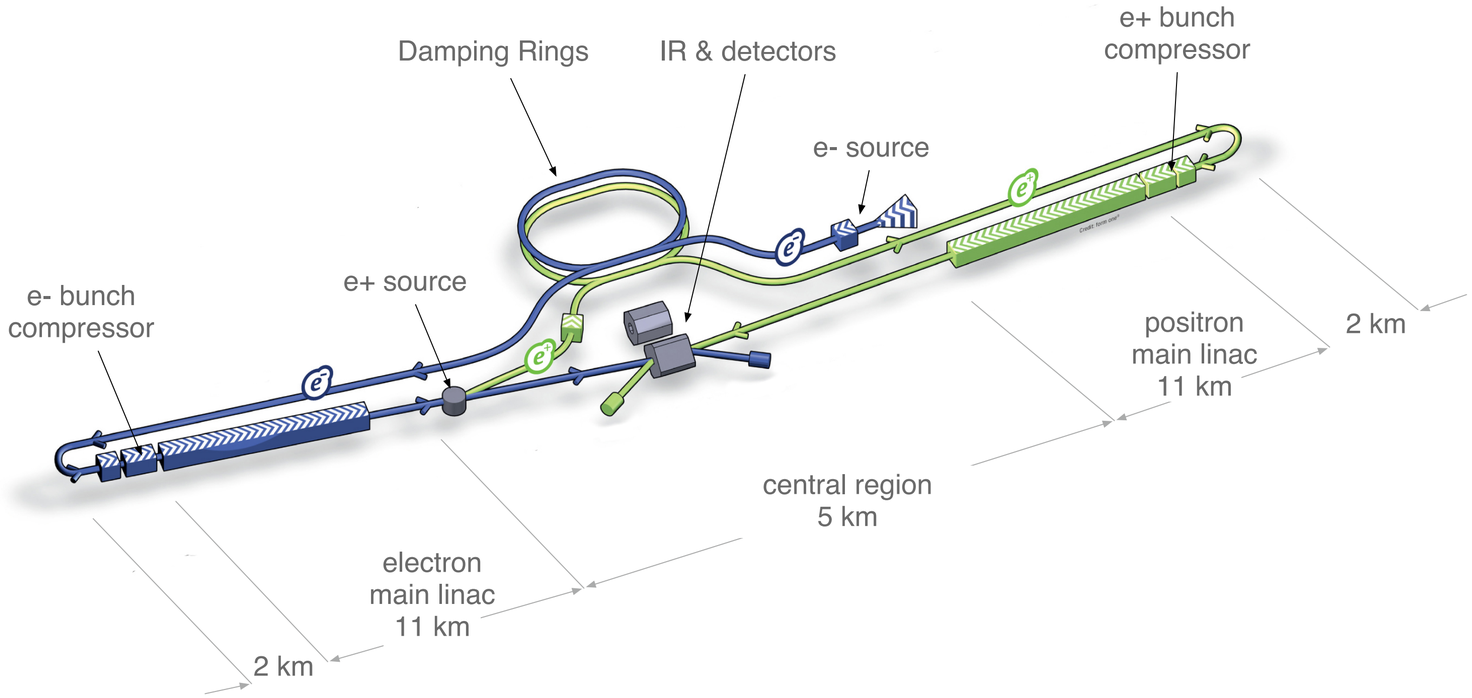
元吉真（T-Micro），SOIPIX R&D グループ

宇宙史構成員会議，2021 年 11 月 26 日

ILC Experiment

ILC Experiment

- e^+e^- linear collider
- Center of mass energy: 250 - 500 GeV (extendable to 1 TeV)
- Precise measurement of the Higgs boson
- Search for physics beyond the Standard Model



ILC TDR vol.4: Detectors
ILD Concept Group, T. Abe et al., arXiv:1006.3396 [hep-ex].

ILC Experiment and Vertex Detector

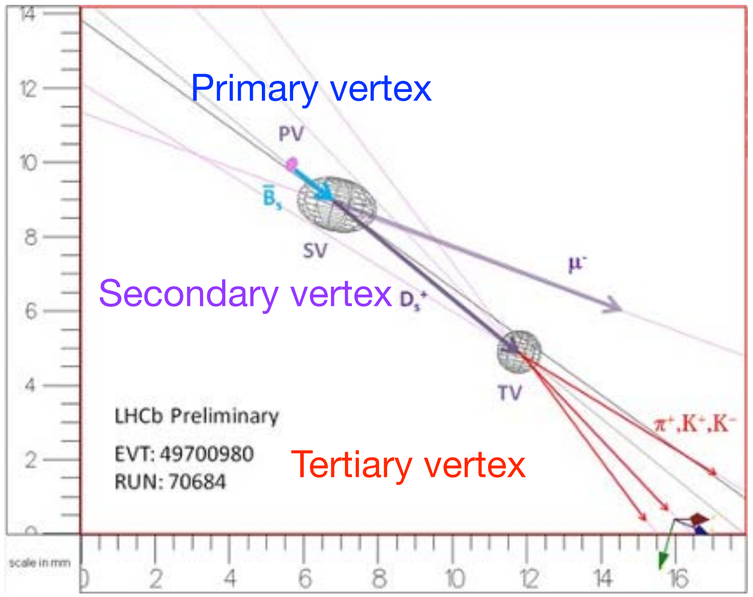
ILC Experiment

- e^+e^- linear collider
- Center of mass energy: 250 - 500 GeV (extendable to 1 TeV)
- Precise measurement of the Higgs boson
- Search for physics beyond the Standard Model

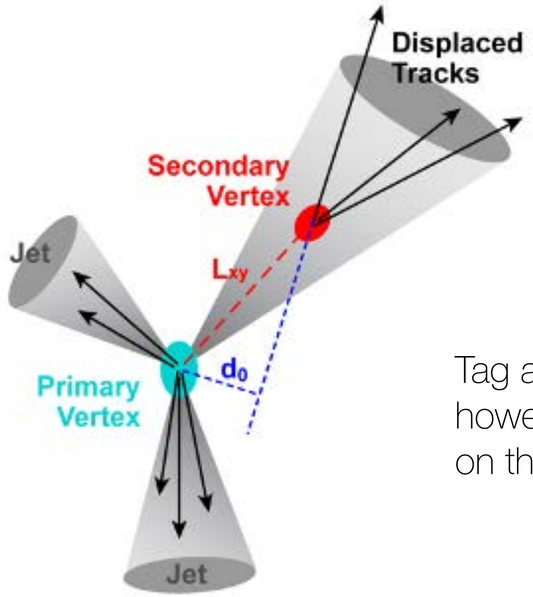
Existence of *b*, *c* quarks and tau lepton in event

Tagging of *b*, *c*, and tau,
reconstruct tracks of daughter charged tracks
interpolate tracks to collision point to reconstruct vertices
→ Displaced vertex and large significance of impact parameter d0 are evidence of existence of *b*, *c*, and tau.

Typically ~10 μm spatial resolution for pixel detector



Ref: LHCb Collaboration



Ref: D0 experiment

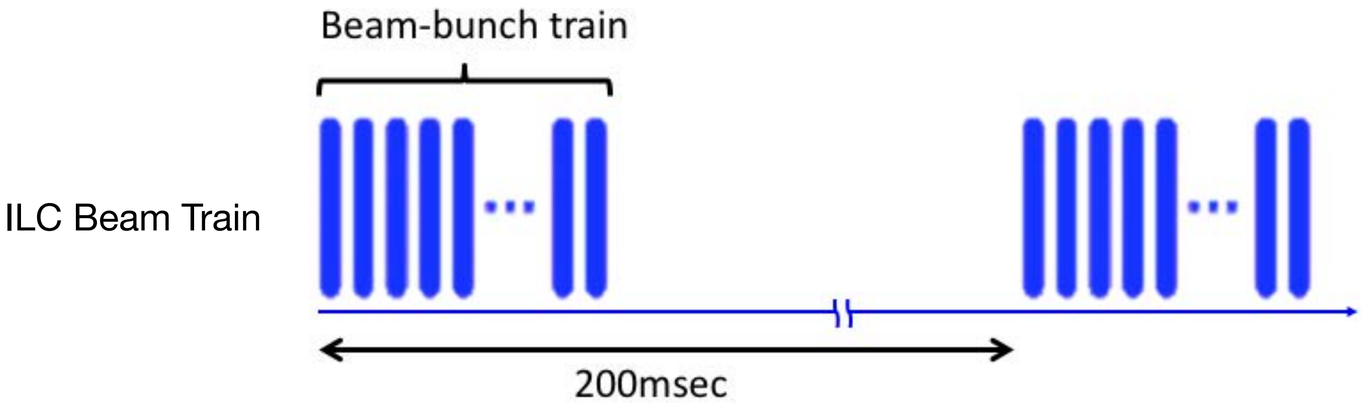
Tag algorithms have been developed in each experiment, however, precision of *b*, *c*, and tau identification depends on the performance of the silicon detectors.

ILC Experiment and Vertex Detector

Requirements:

1) Single point resolution: better than 3 μm
   Pixel size: ~20 × 20 μm^2
2) Time resolution: single-crossing (554 ns interval) time resolution
3) Detector occupancy: < 2 %
4) Low material budget: $X \leq 0.1 - 0.2\ \%\ X_0$ / Layer
   corresponds to ~ 100 - 200 μm Si, (supports, cables and cooling add further material)
   low-power ASICs (~ 50 mW/cm^2) + gas-flow cooling
5) Radiation hardness:
   TID : < 1 kGy / year
   NIEL: < 10^{11} 1MeV n_{eq} / cm^2 / year

~1,300 bunches (every 554 ns)



ILC TDR v4 Detector
LC Vertex / Tracking R&D 2nd Nov. 2015

SOI Pixel Sensor

SOI: Silicon-on-Insulator technology

Utilize 0.2 μm FD-SOI CMOS process by
Lapis Semiconductor Co. Ltd.

SOI Pixel Detector: Monolithic type detector

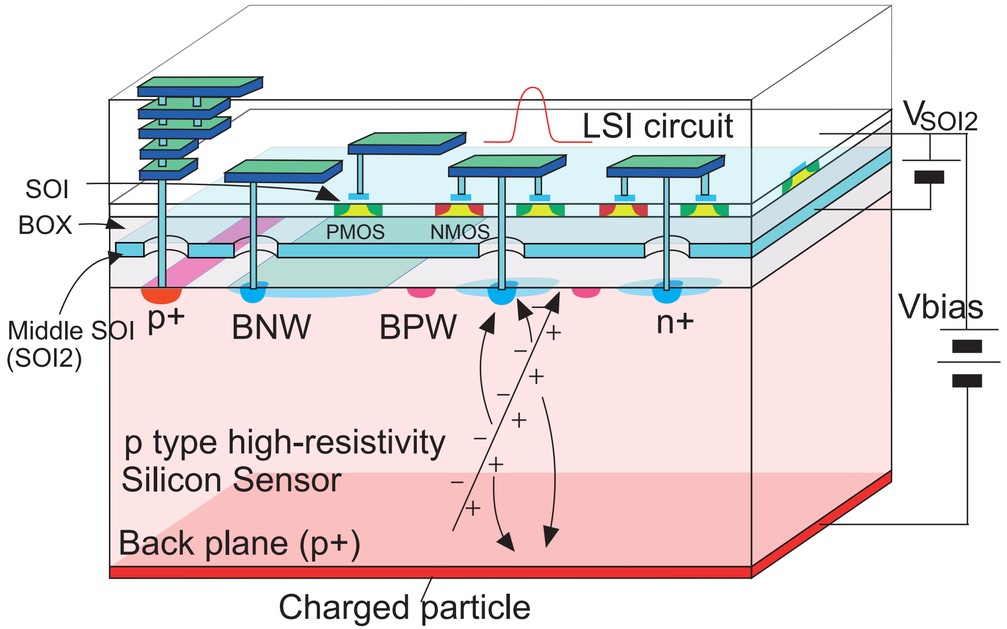
- LSI is processed on Buried Oxide layer (BOX)
- Smaller pixel size, complex circuit in pixel
- Low material budget
- High speed, low power
- Less single event effects (SEE) probability
- Low cost

Double SOI Pixel Detector

Middle Si layer suppresses

- Back gate effect
- Sensor-Circuit cross talk
  - Middle Si layer shields coupling between sensor and circuit.
  - It is useful for analog and digital mixed circuit in pixel.
- Radiation damage (TID)
  - It is able to compensate electric field generated by trapped holes in the BOX.
  - It can be used in high radiation environment (~1MGy).
  - (K. Hara, Vertex2017, Sep. 11-15, 2017, Las Caldas)

Double SOI Pixel Detector



Illustrated by T. Tsuboyama (KEK)

Sensor thickness: 50 - 500 μm
Sensor Resistivity: > 1 kΩ·cm
SOI2 thickness: 150 μm (*n*-type)
SOI2 Resistivity: < 10 Ω·cm

Architecture of SOFIST

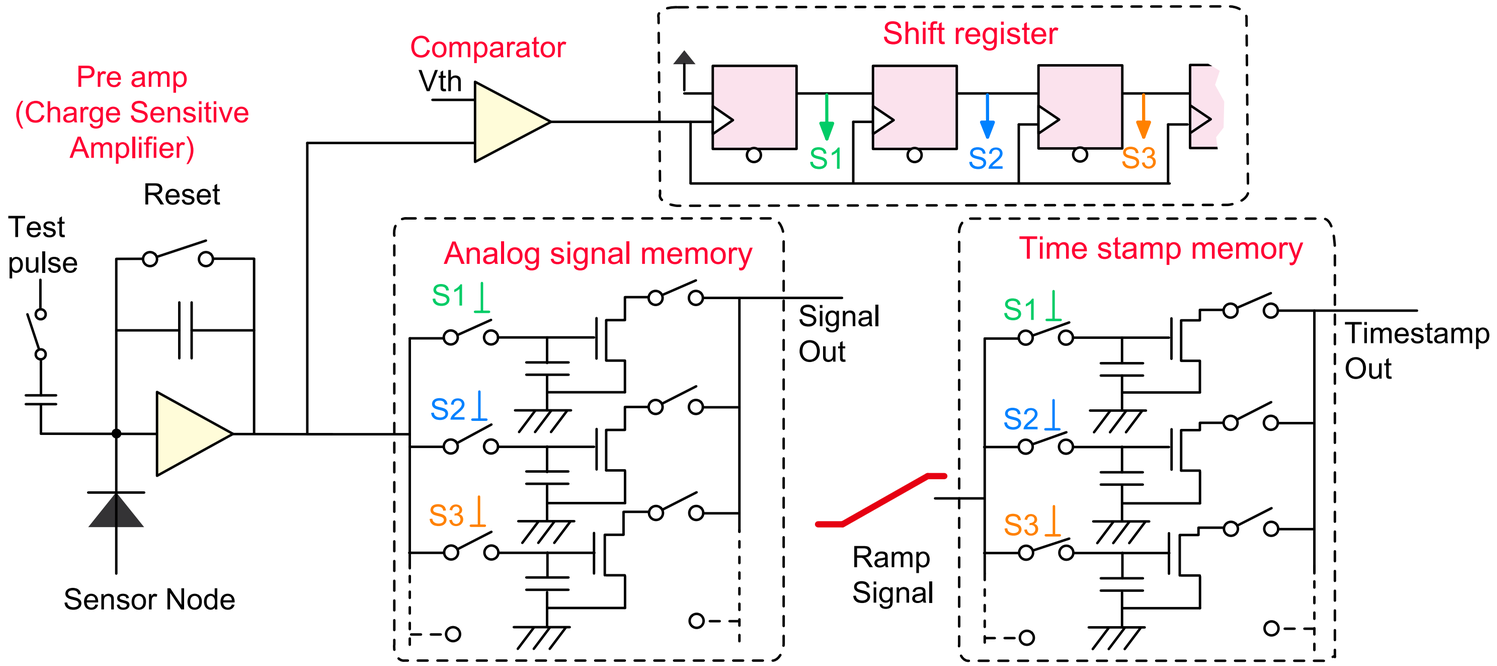
In a Pixel

- **Pre-amplifier**
- **Comparator**
  Keep the analog signal and time stamp if a signal exceeds a threshold V_{th}.
- **Shift register (Hit memory)**
  Latch for multiple memories.
- **Analog signal memory**
  Store signal charges up to two (or more) hits.
- **Time stamp circuit**
  Store time stamps up to two (or more) hits.

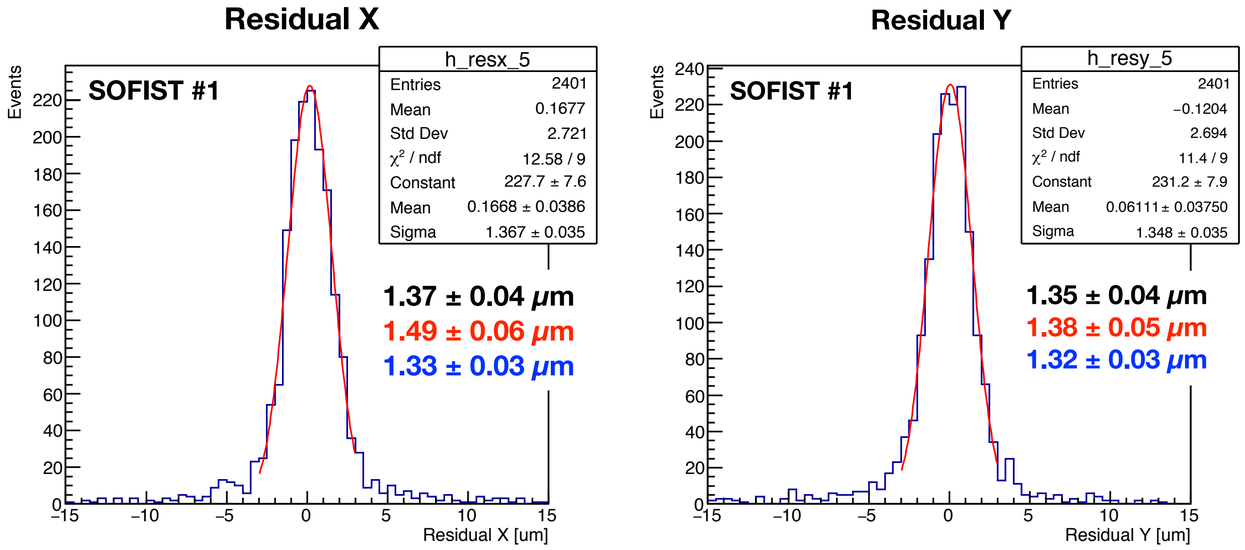
On Chip

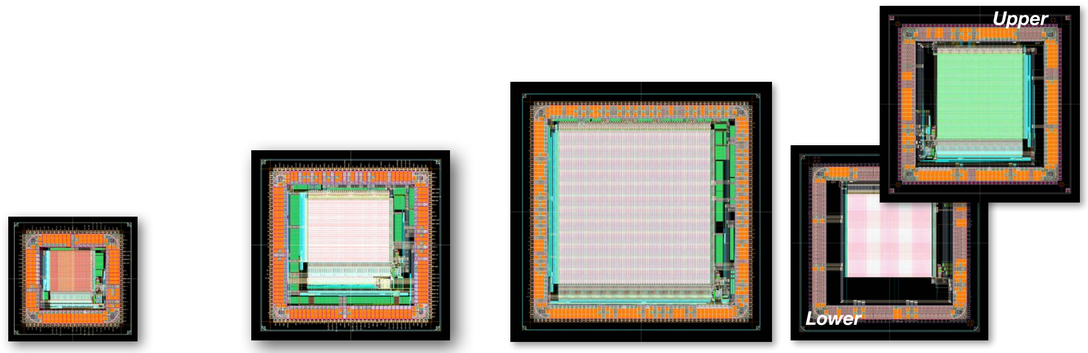
- **Column ADC**
  Digitize analog signal and time stamp.
- **Zero-Suppression logic**
  Extract hit pixels and reduce the data to transfer to backend.

SOFIST Pixel Circuit



SOFIST1





SOFIST1
Position resolution
σ~1.4 μm

SOFIST2
Time resolution
σ~1.55 μs

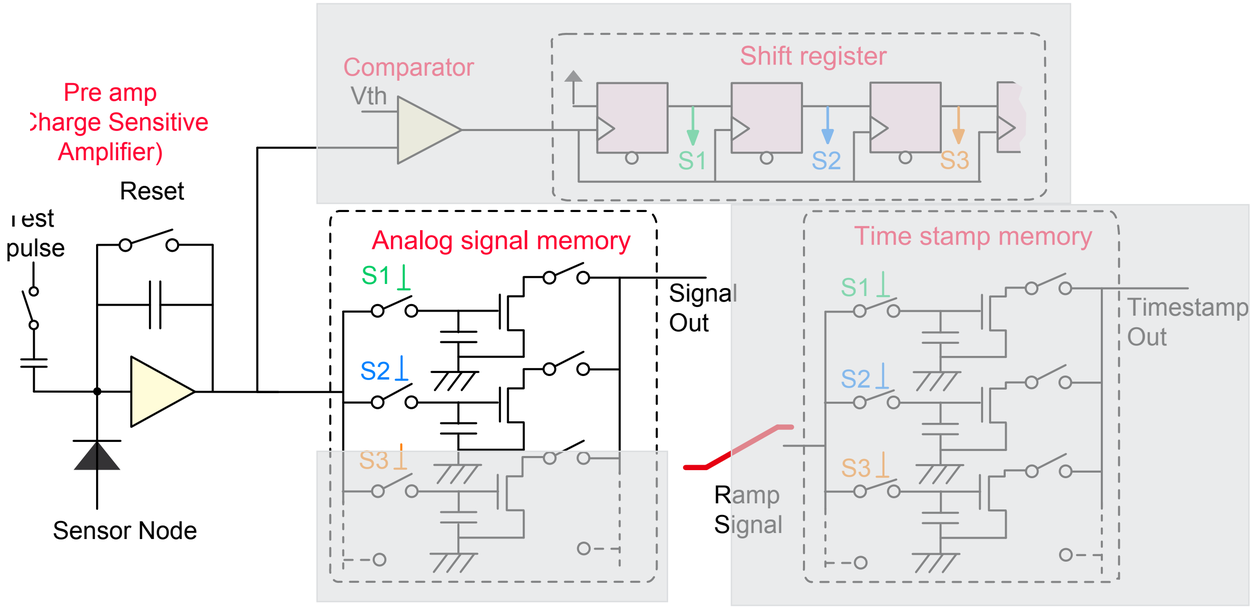
SOFIST3
Full function
(30×30 μm² pixel)

SOFIST4
Full function
(20×20 μm² pixel)

Sensor Thickness: 500 μm

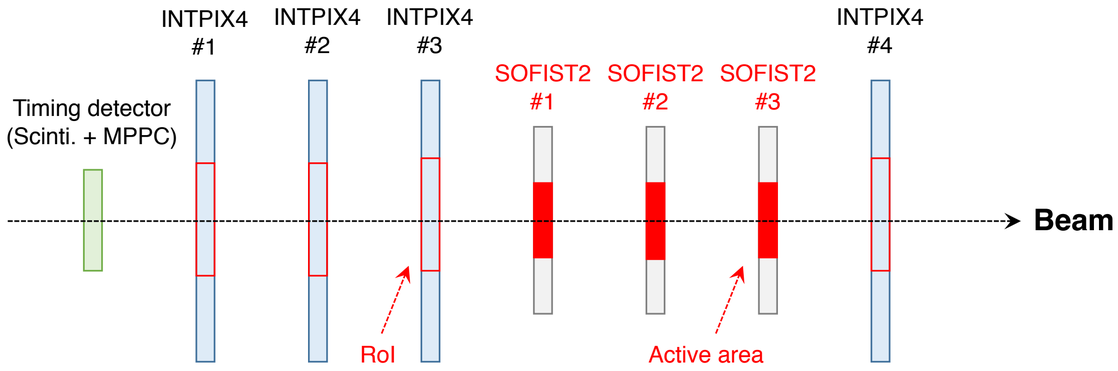
Readout and Sensor depletion layer

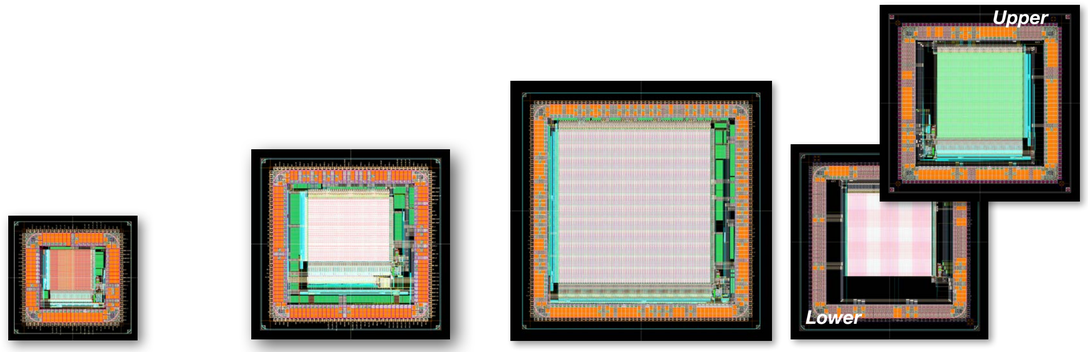
12-bit external ADC, 500 μm (Full depletion)
8-bit on-chip ADC, 500 μm (Full depletion)
12-bit external ADC, 200 μm (Partial depletion)



SOFIST2

Sensor Thickness: 65 μm





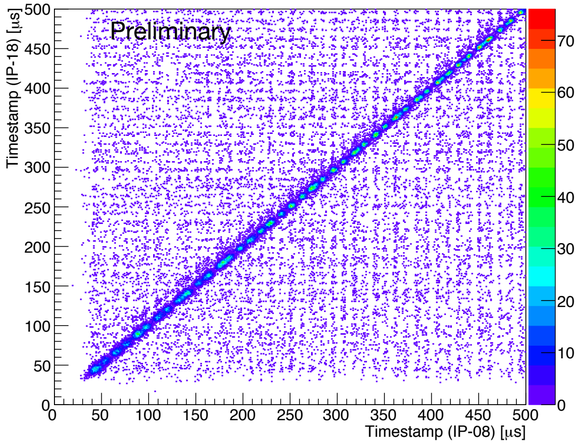
SOFIST1
Position resolution
σ~1.4 μm

SOFIST2
Time resolution
σ~1.55 μs

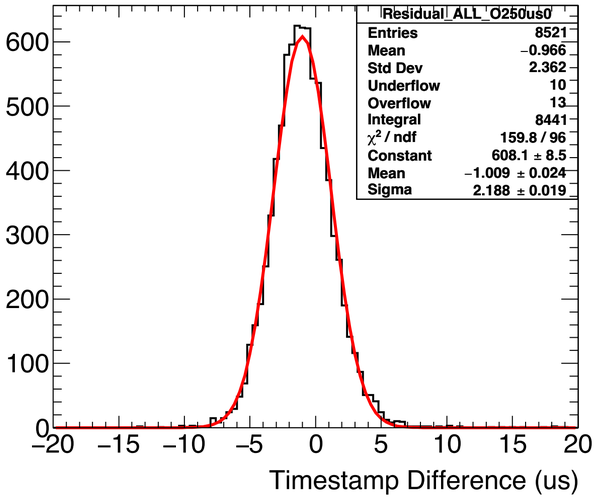
SOFIST3
Full function
(30×30 μm² pixel)

SOFIST4
Full function
(20×20 μm² pixel)

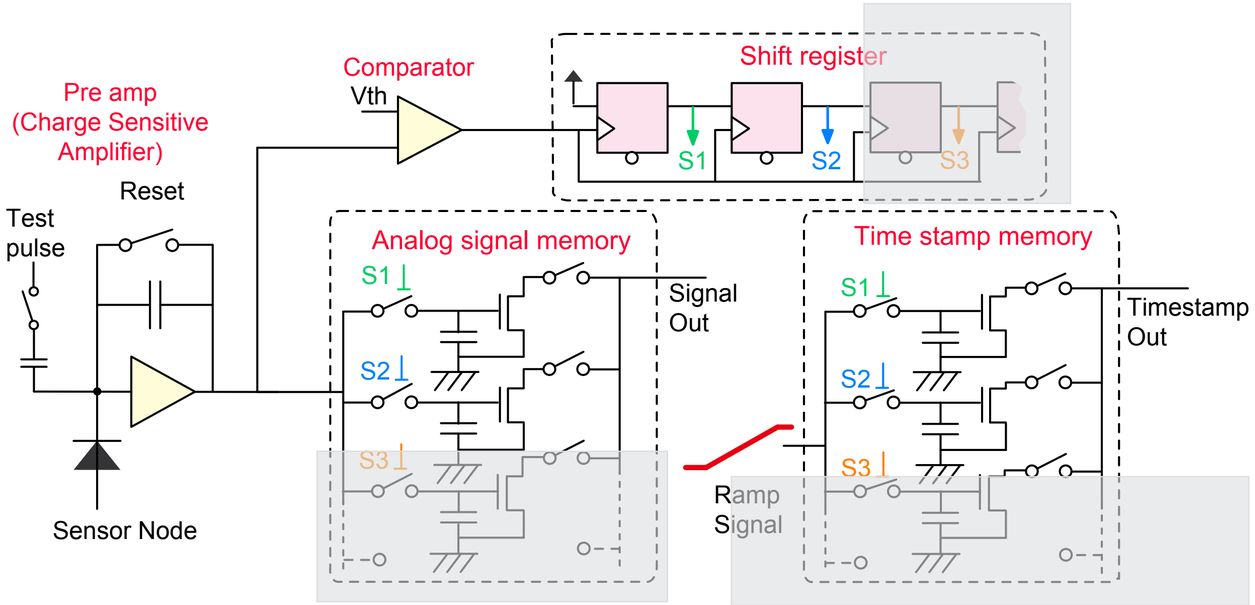
Timestamp correlation between SOFIST ver.2 #1 and #2



Timestamp difference between SOFIST ver.2 #1 and #2

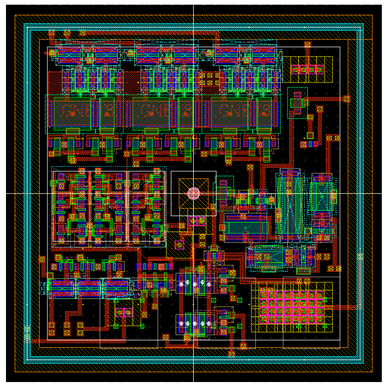


Intrinsic resolution: 2.19/√2 ~ 1.55 μs



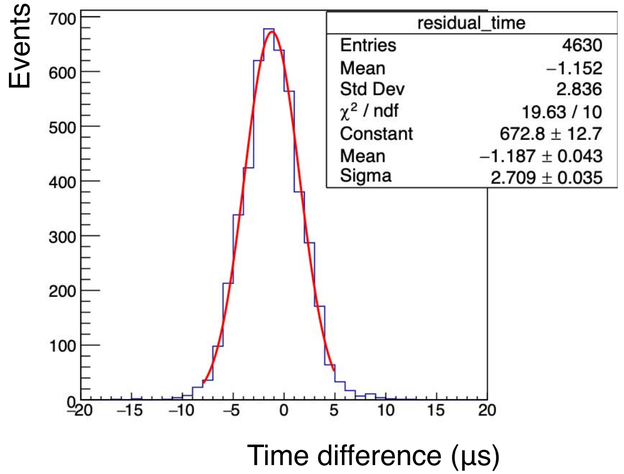
SOFIST3

Pixel size: 30 × 30 μm²



Timestamp residual

Timestamp difference between #1 and #4.

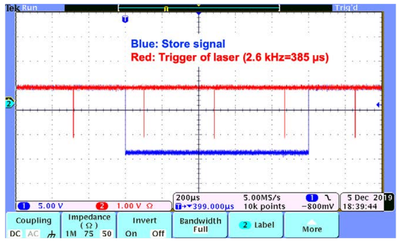


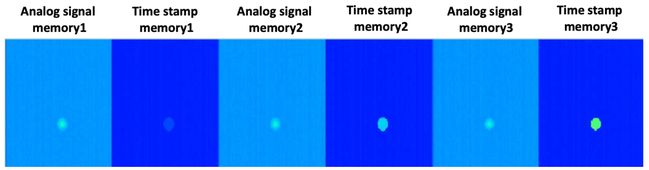
Intrinsic resolution: 2.71/√2 ~ 1.92 *μs*

Sensor Thickness: 300 μm

Multi-memory readout test

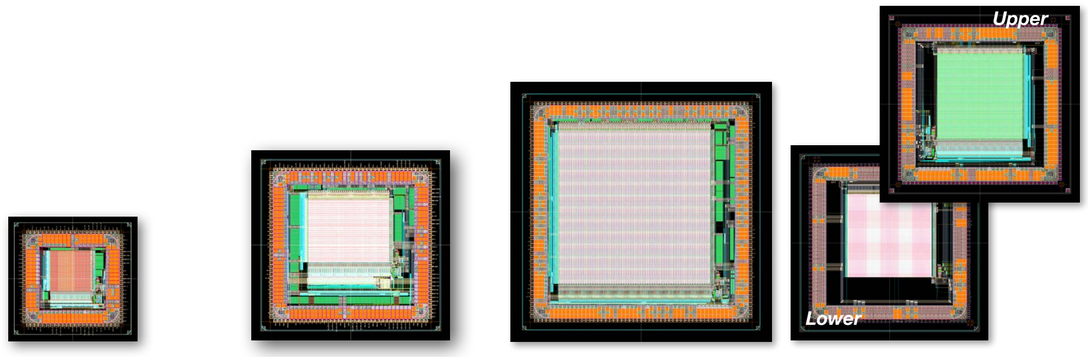
SOFIST3 has three hit, analog signal and timestamp memories.
Multi-memory readout scheme was tested by injecting a IR laser three times in a 1 ms period.





Analog signal
Represent stable laser pulses (~180 ADC).

Timestamp
Show different timing of the laser injection (110, 490, 880 ADC).

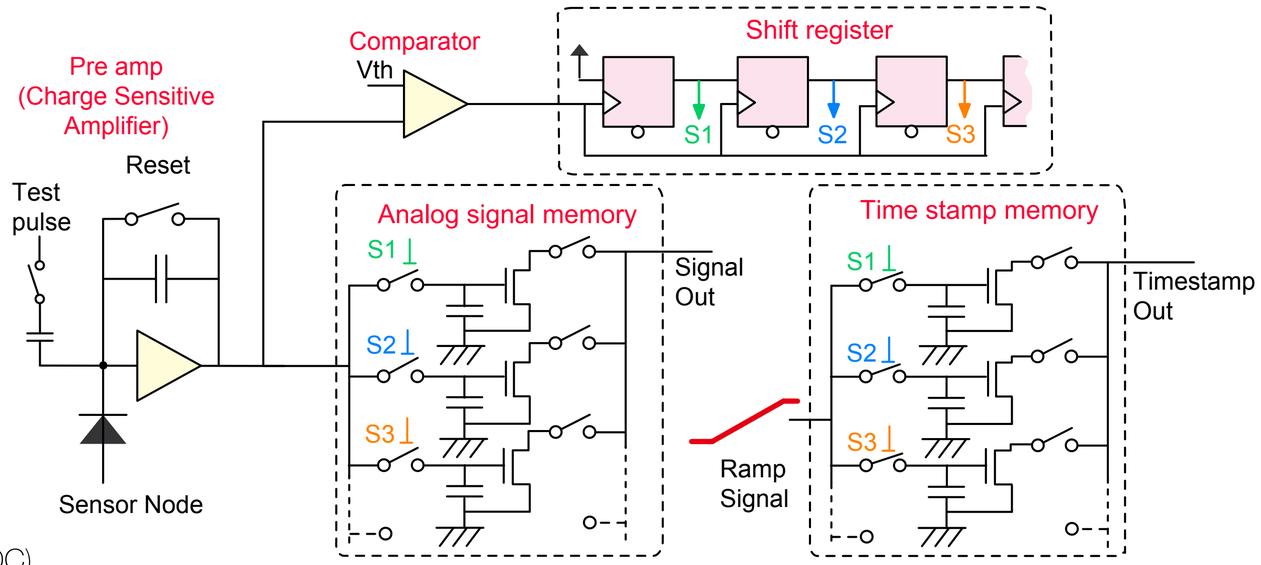


SOFIST1
Position resolution
σ~1.4 μm

SOFIST2
Time resolution
σ~1.55 μs

SOFIST3
Full function
(30×30 μm² pixel)

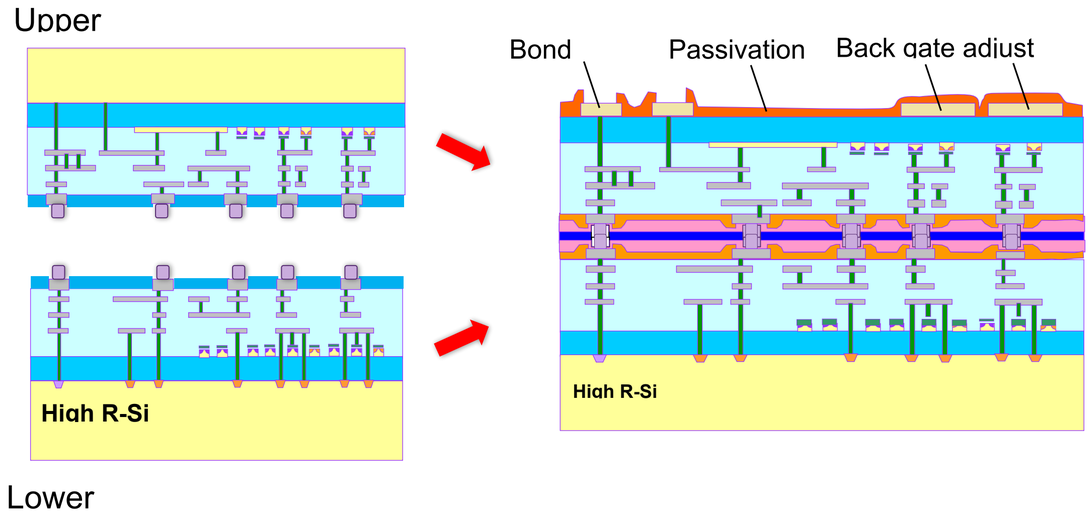
SOFIST4
Full function
(20×20 μm² pixel)

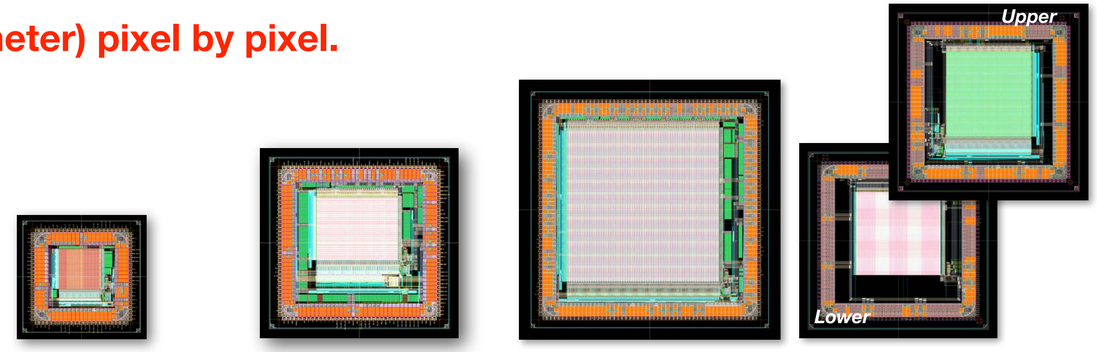


SOFIST4

by Tohoku-Micro Tec (T-Micro), M. Motoyoshi
http://www.t-microtec.com

Two SOFIST4 chips (lower and upper) are connected by **micro bump (3 μm diameter) pixel by pixel.**
→ Keep pixel size small and implement complex circuit three dimensionally.



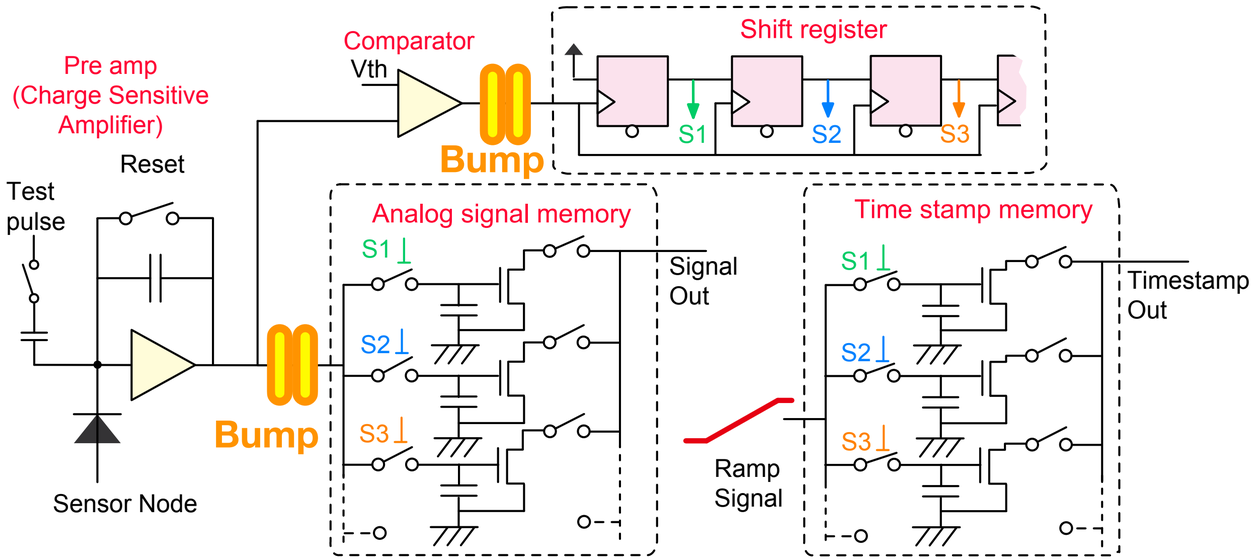


SOFIST1
Position resolution
σ~1.4 μm

SOFIST2
Time resolution
σ~1.55 μs

SOFIST3
Full function
(30×30 μm² pixel)

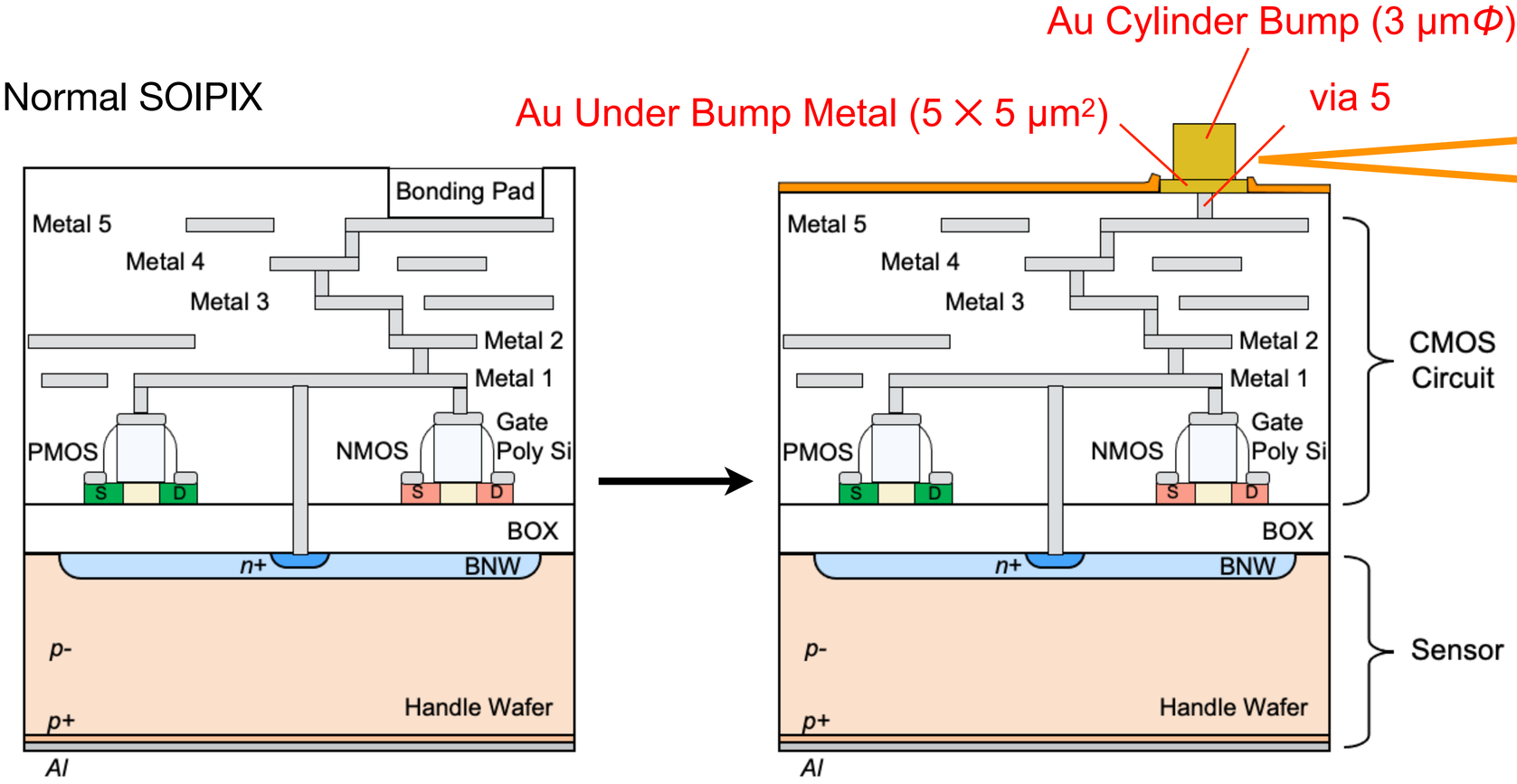
SOFIST4
Full function
(20×20 μm² pixel)

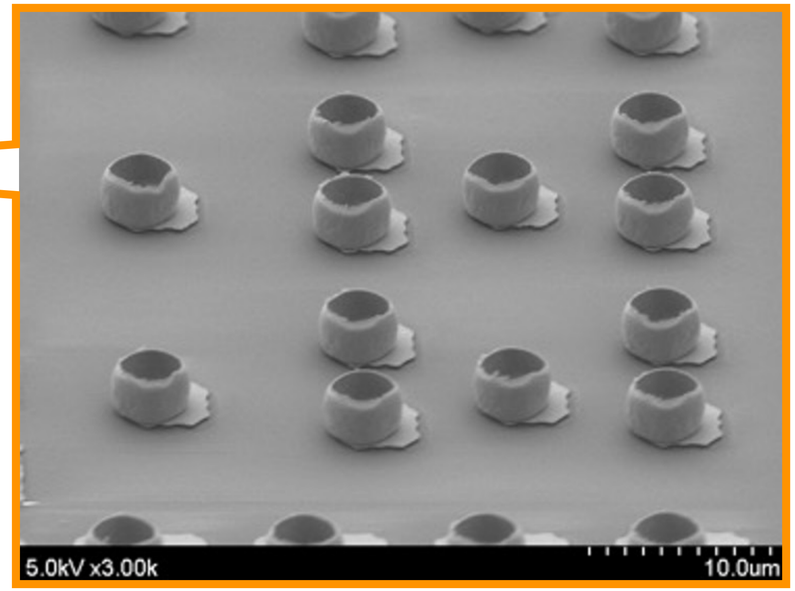


Lower Chip (Pixel):
Used as sensor and implement analog circuit in a pixel.
Upper Chip (Pixel):
Sensor layer is removed by wet etching and then formed Al pad for wire bonding on the BOX.
Digital circuits/memories are implemented in a pixel.

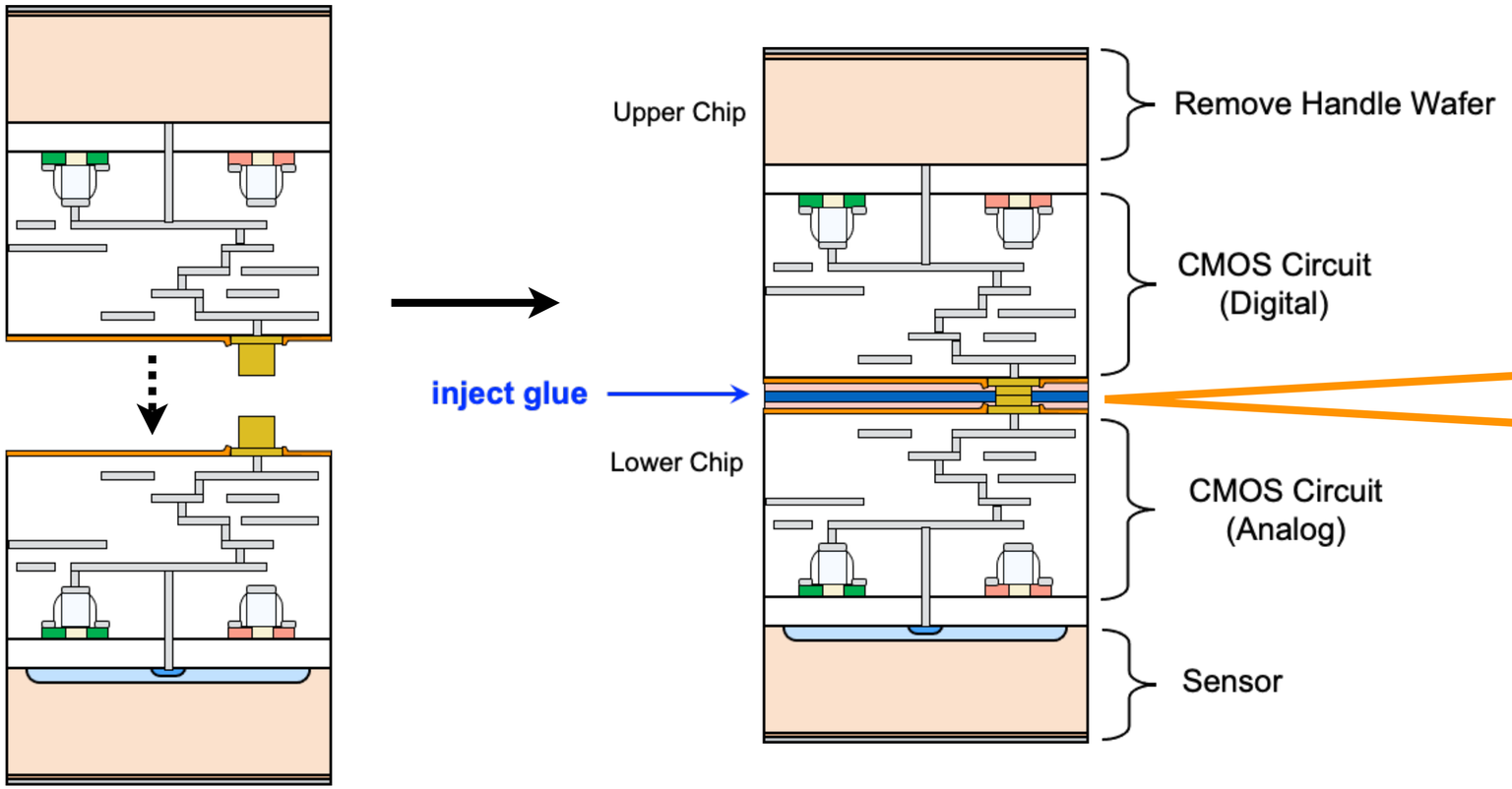
SOIPIX 3D Stacking Technology

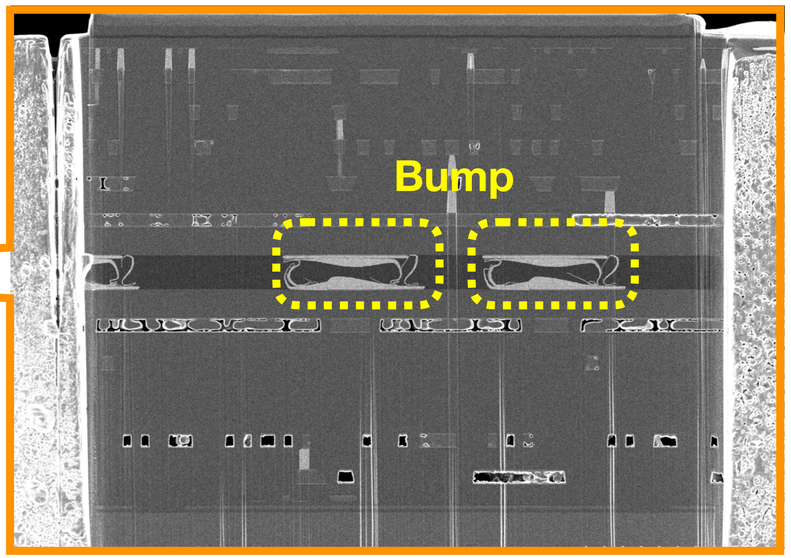
Normal SOIPIX



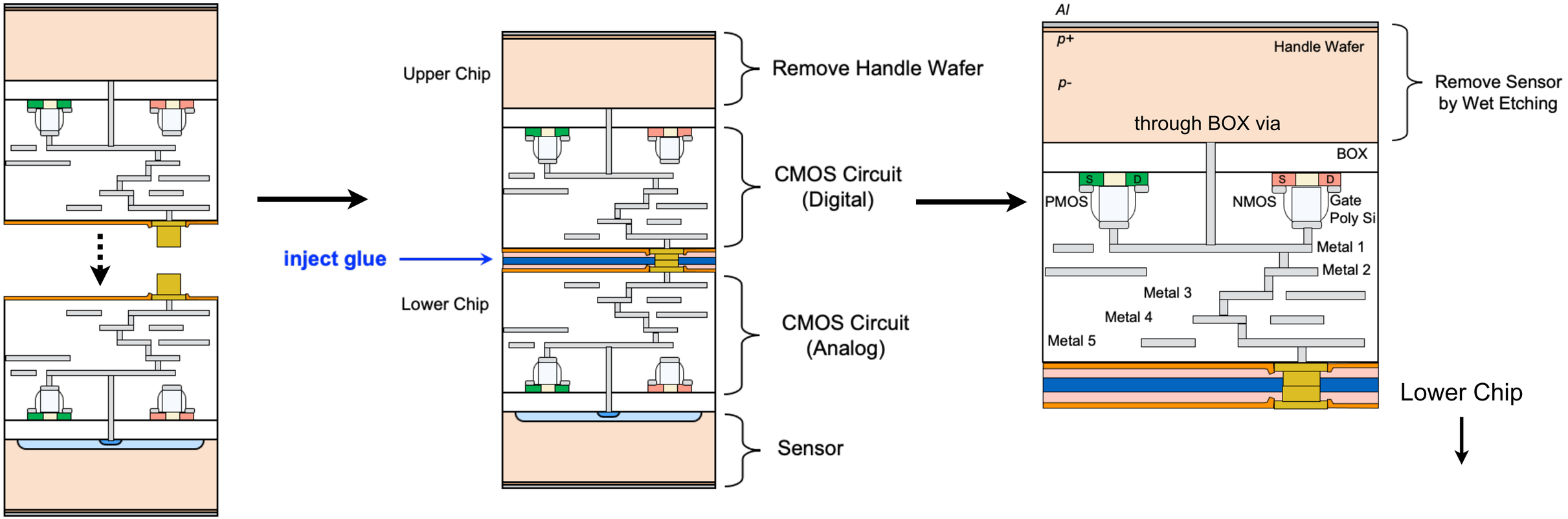


SOIPIX 3D Stacking Technology

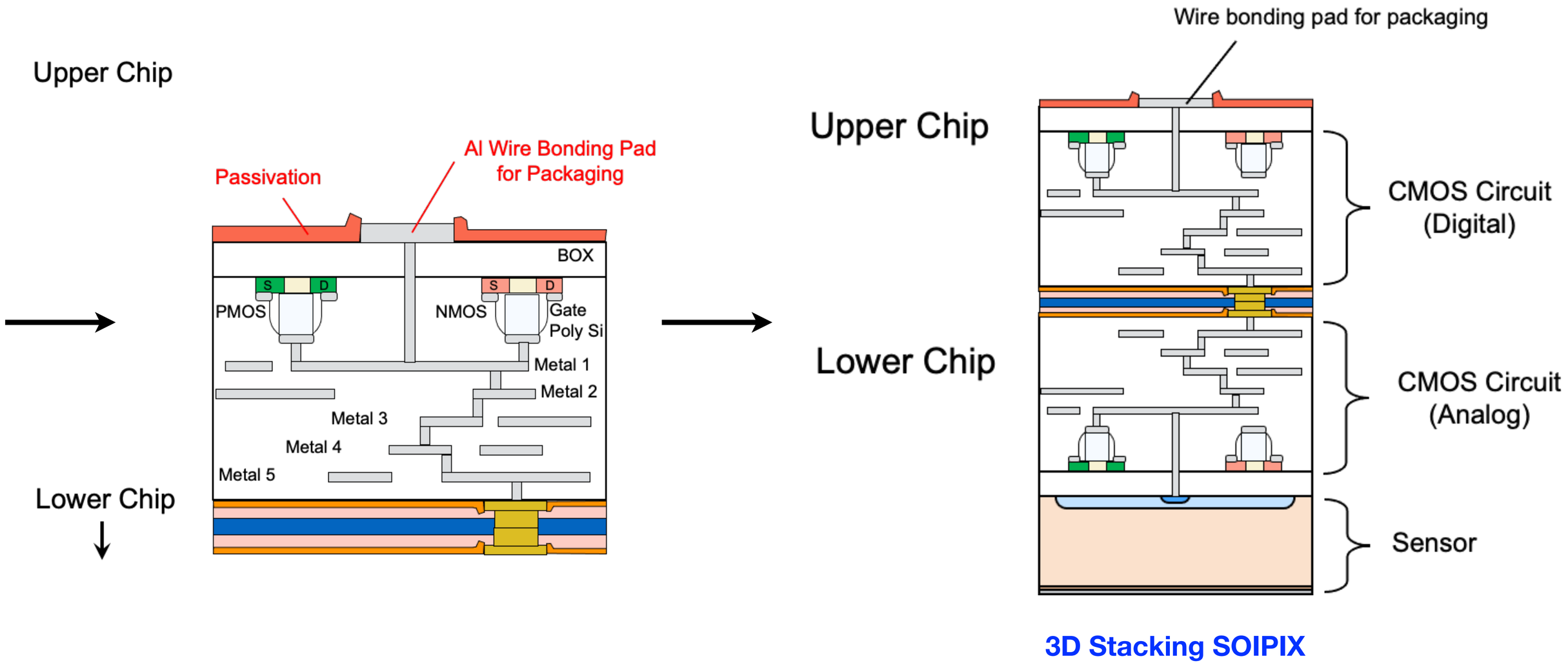




SOIPIX 3D Stacking Technology



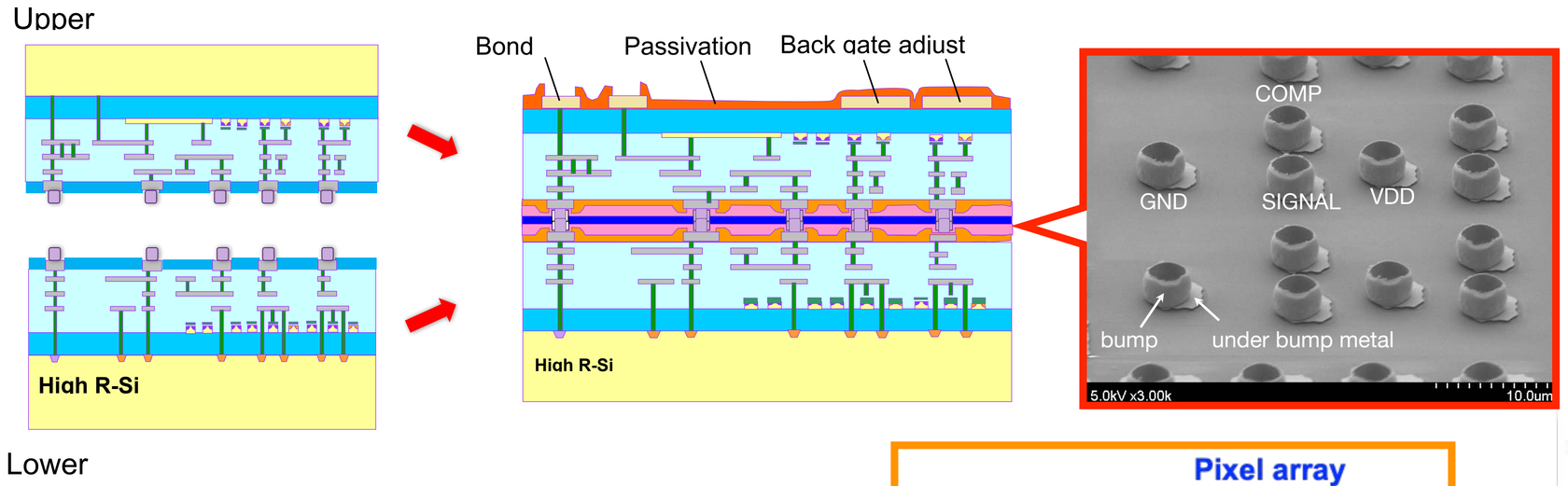
SOIPIX 3D Stacking Technology



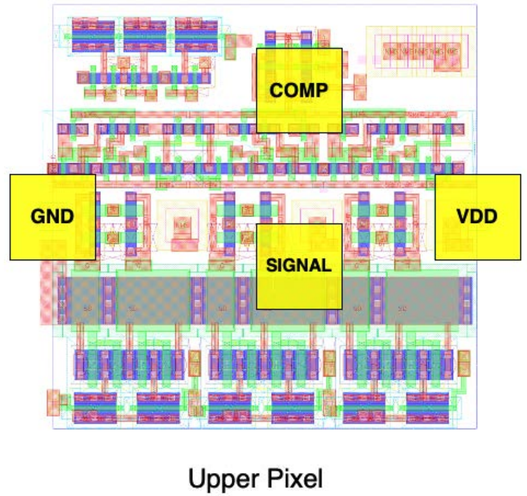
3D Stacking SOIPIX

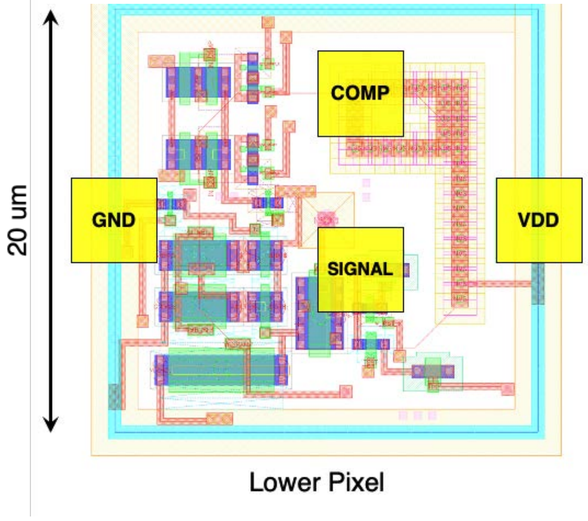
SOFIST4

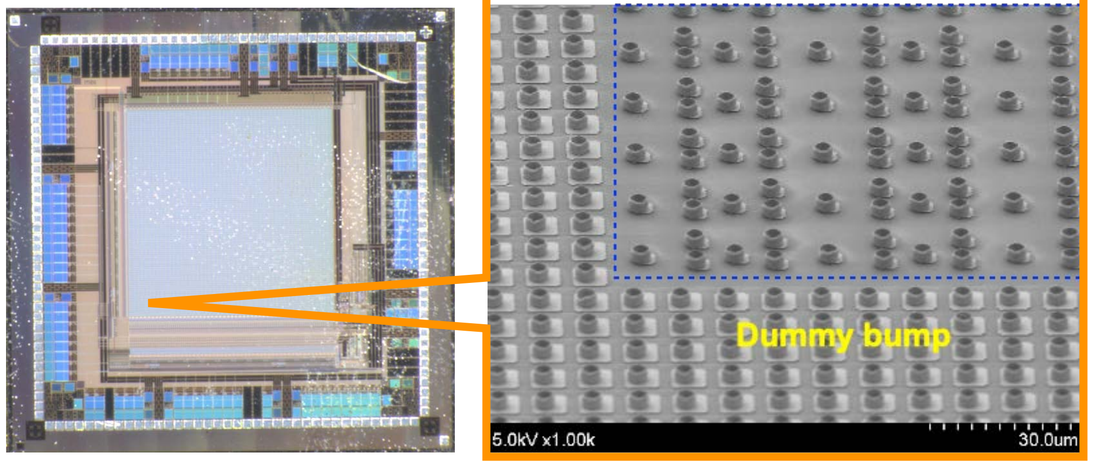
Two SOFIST4 chips (lower and upper) are connected by micro bump (3 μm diameter) pixel by pixel.
→ Keep pixel size small and implement complex circuit three dimensionally.



Lower and Upper Pixel Layout





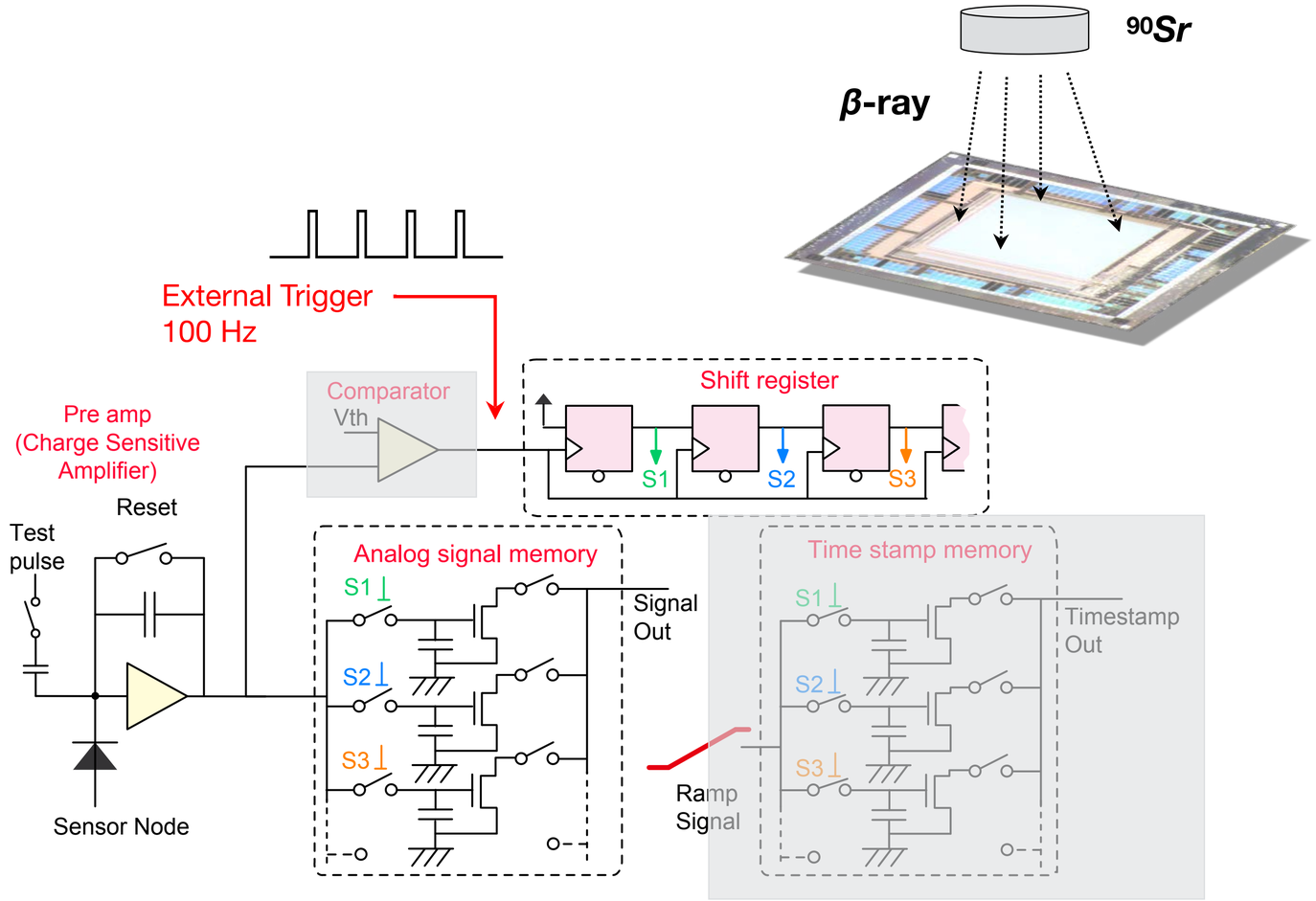


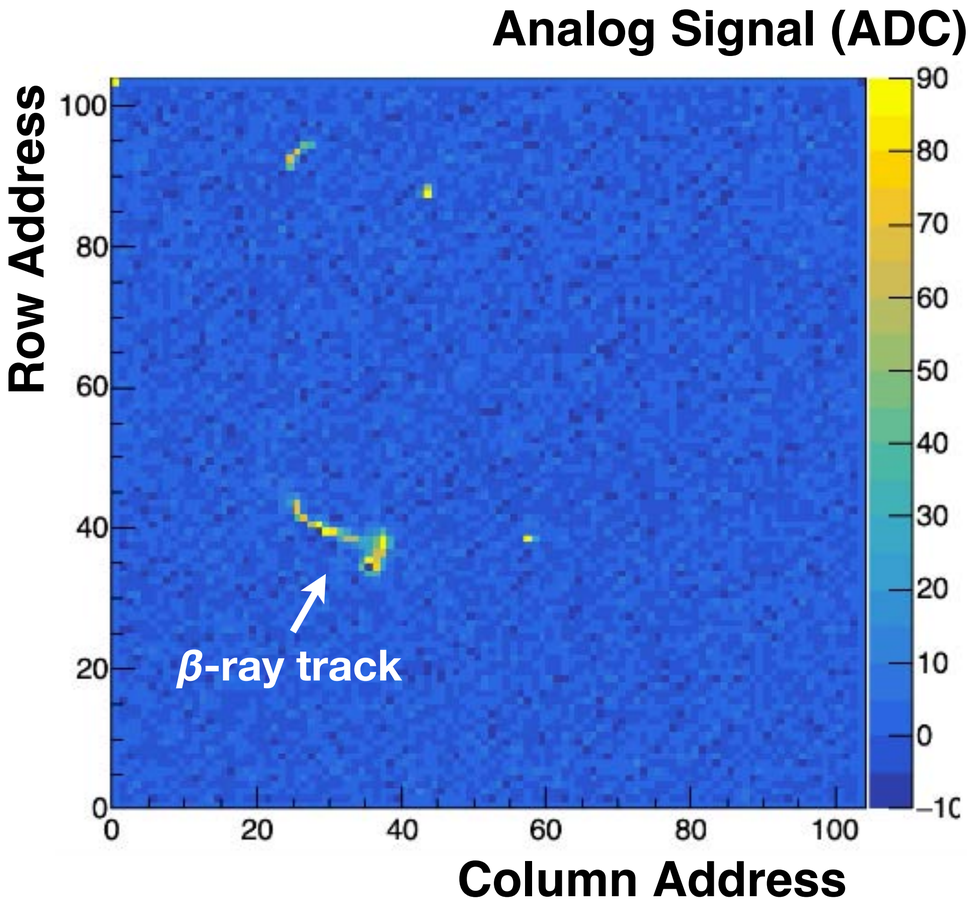
SOFIST4 Chip

- Chip size: 4.45 × 4.45 mm^2
- Pixel size: 20 × 20 μm^2
- Active area: 2.08 × 2.08 mm^2
- Sensor type: FZ p-type
- Sensor thickness: 300 μm
- Sensor resistivity: 3 – 10 kΩ・cm

SOFIST4, β-ray track

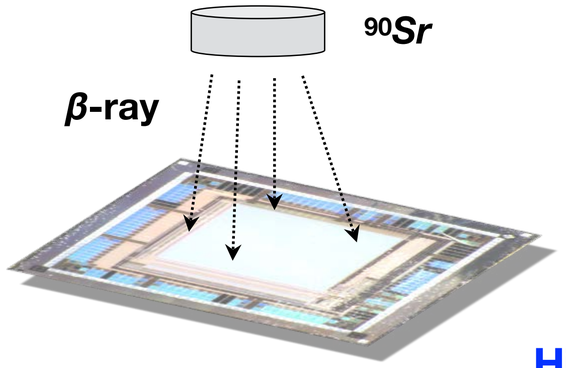
*The sensors we have evaluated were single-SOI FZ-n type sensor due to the process issue of the 3D stacking.
→Comparator, Shift-register and Timestamp functions does not work at this time.

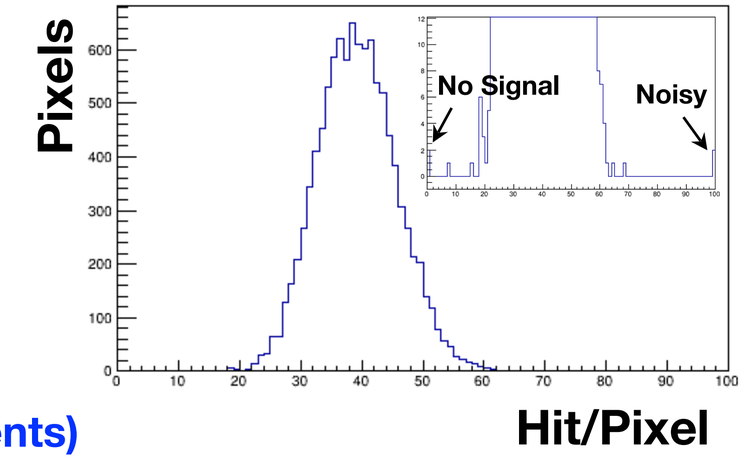


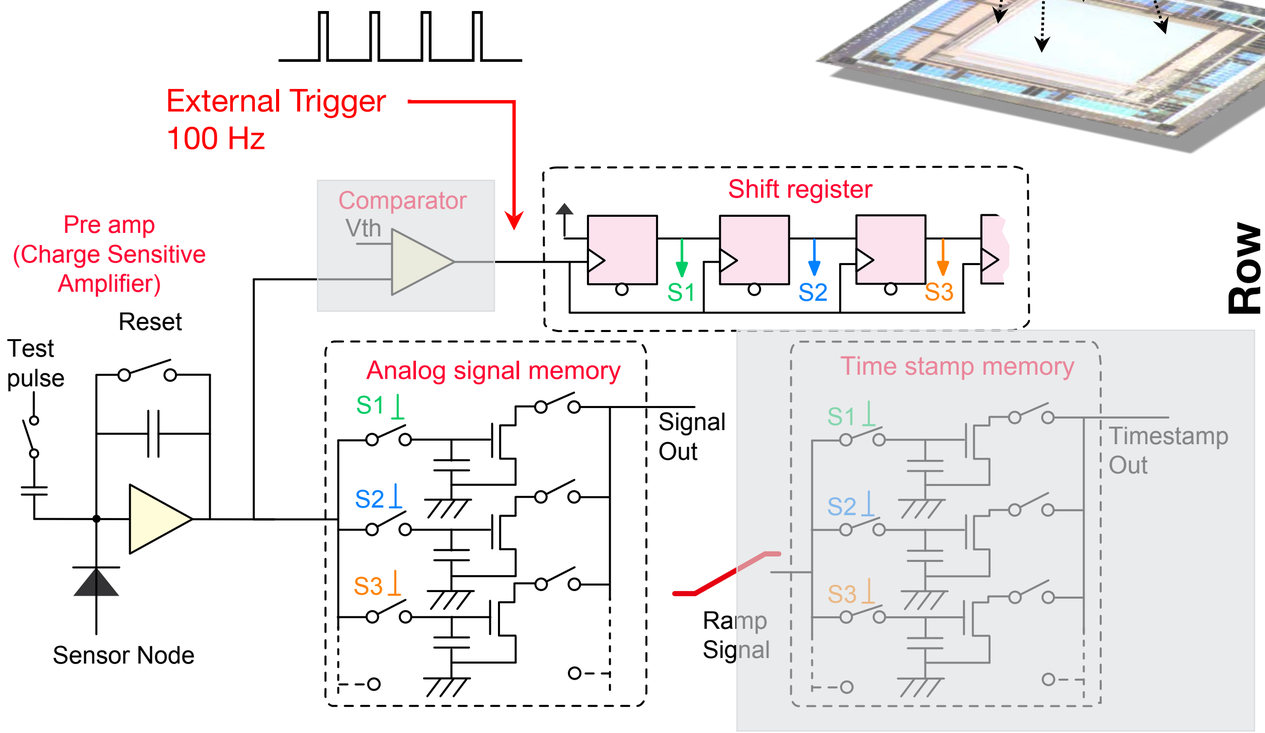


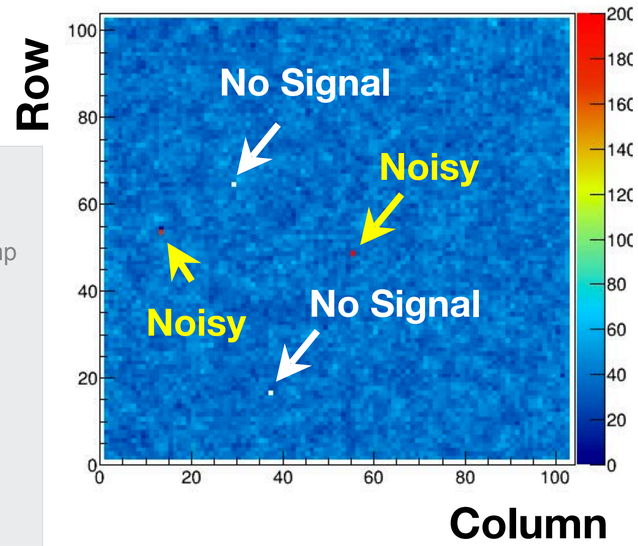
SOFIST4, Bump Connection Yield

*The sensors we have evaluated were single-SOI FZ-n type sensor due to the process issue of the 3D integration.
→Comparator, Shift-register and Timestamp functions does not work at this time.









Connection Yield:
(102 × 102 – 2) / 102 × 102
~ 99.98 %

Reject the outermost pixels for the calculation.

Beam Test

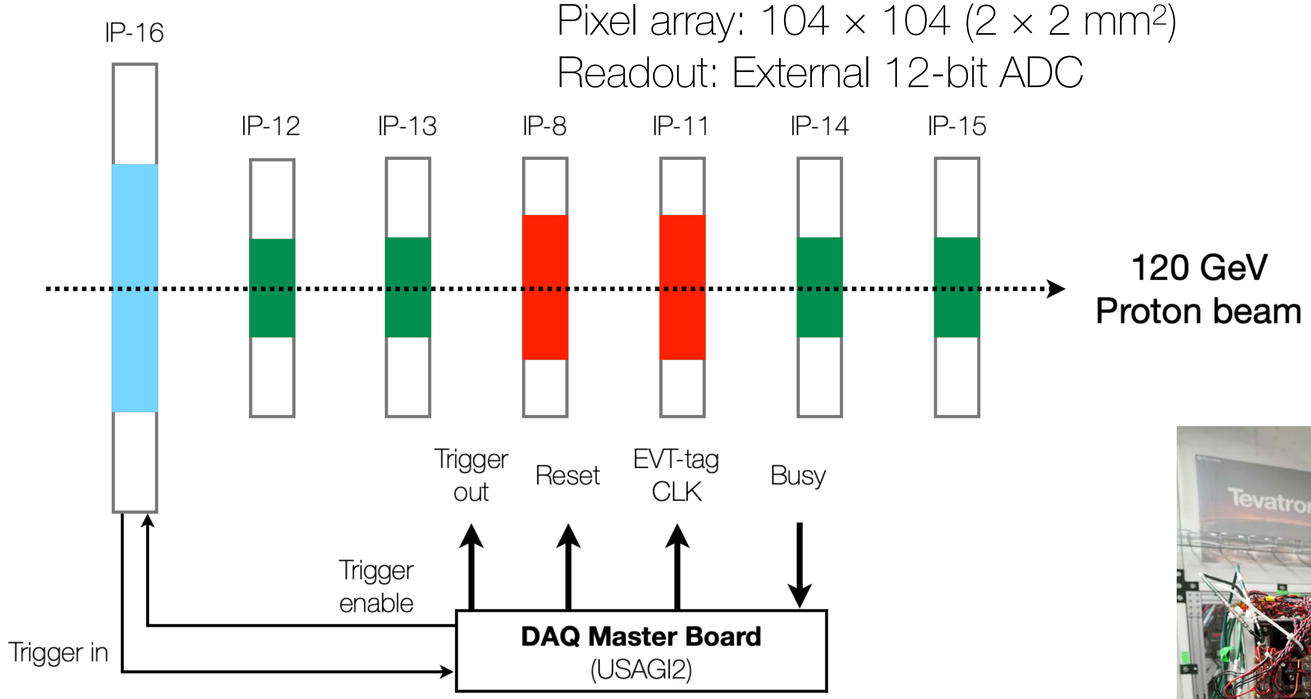
Beam: 120 GeV proton (Fermilab Beam Test Facility)
DAQ rate: ~120 events/s

SOFIST4

Pixel size: 20 × 20 μm²
Pixel array: 104 × 104 (2 × 2 mm²)
Readout: External 12-bit ADC

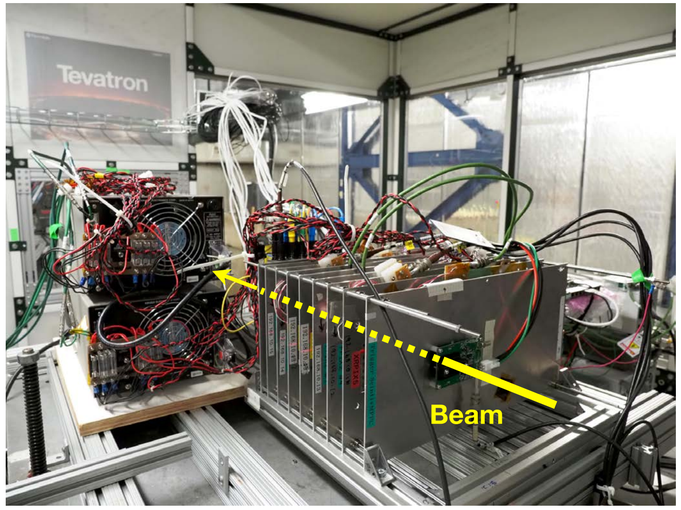
FPIX2 (SOIPIX)

Telescope for SOFIST
σ ~0.7 μm
Pixel size: 8 × 8 μm²
Pixel array: 128 × 128 (1 × 1 mm²)
Readout: External 12-bit ADC



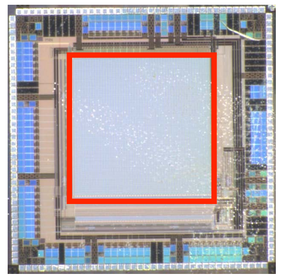
XRPIX5 (SOIPIX)

Trigger counter
Pixel size: 36 × 36 μm²
Pixel array: 608 × 384 (24.6 × 13.8 mm²)
Region of Interest function
Readout: External 12-bit ADC

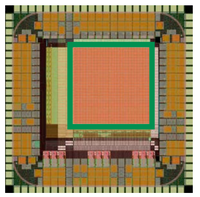


* **Active area:** FPIX2: 1 × 1 mm², SOFIST4: 2 × 2 mm²

SOFIST4



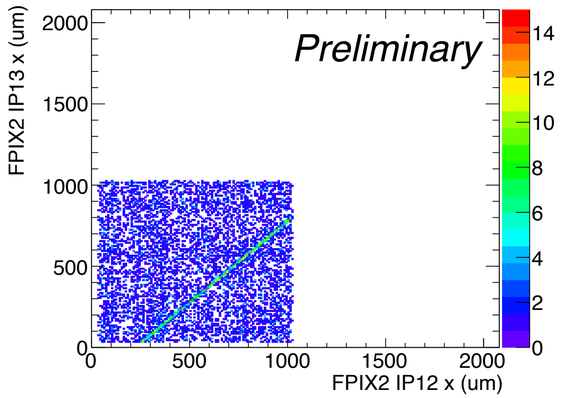
FPIX2

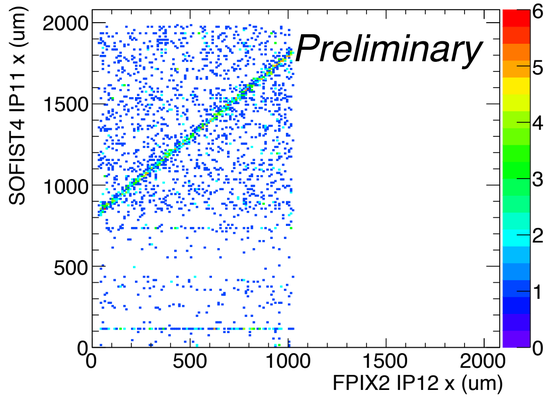


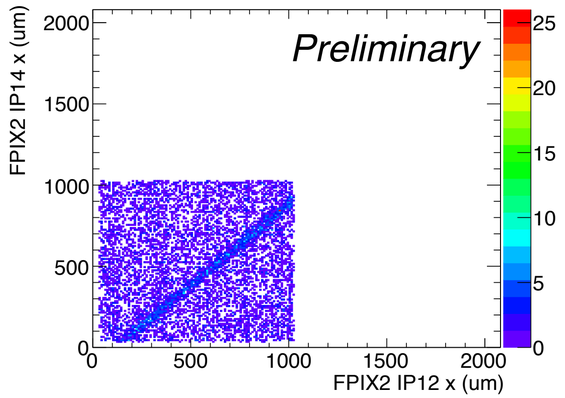
Hit Correlation

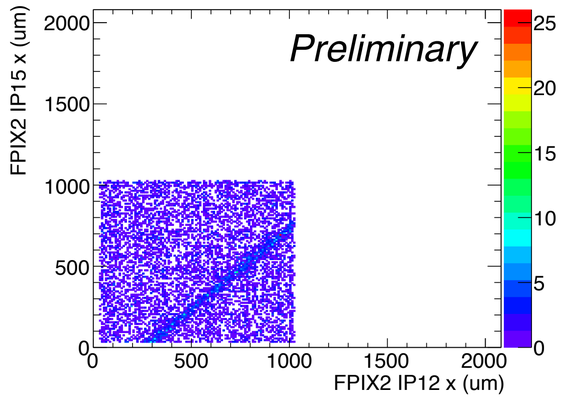
Hit position correction between **telescope (FPIX2) and SOFIST4 IP-11** in *x* and *y*-direction.

x-direction

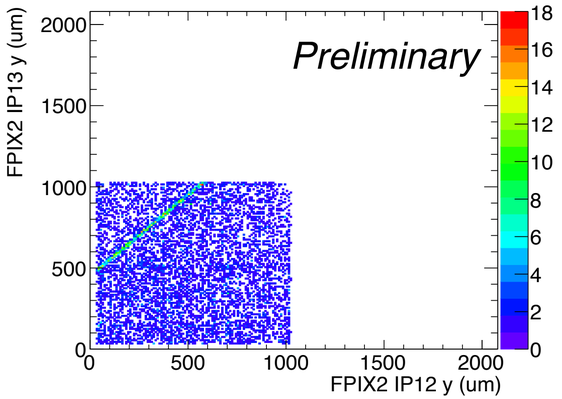


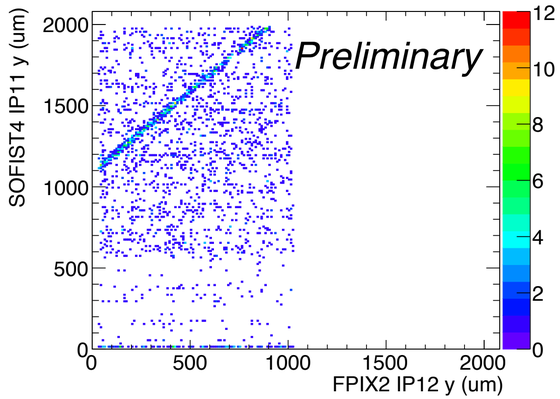


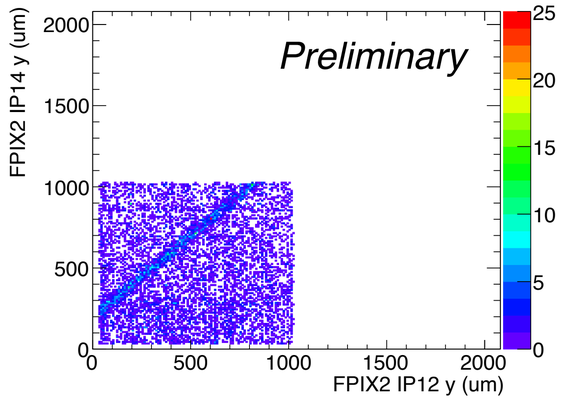


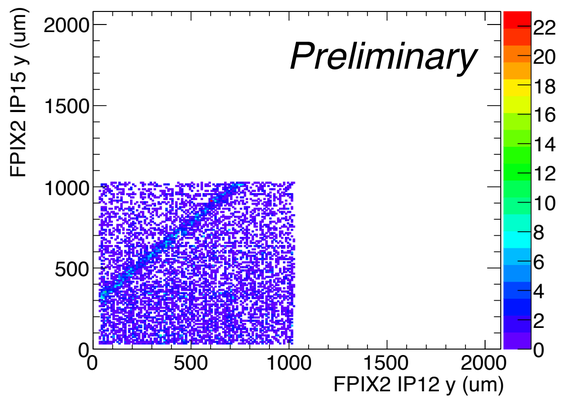


y-direction



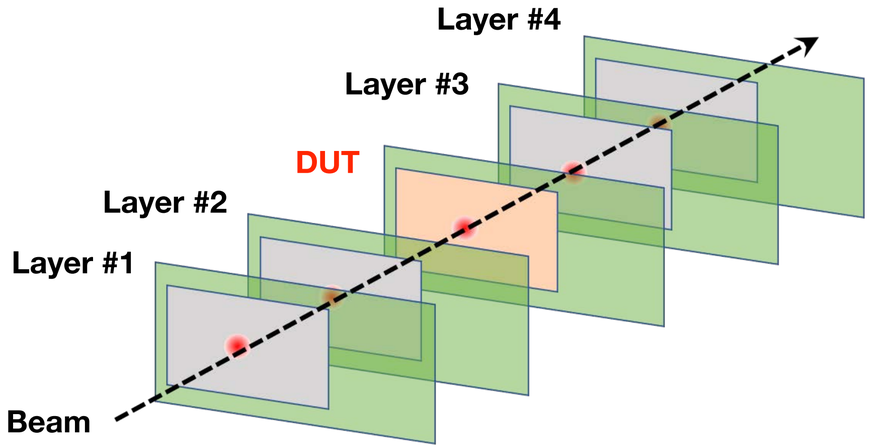




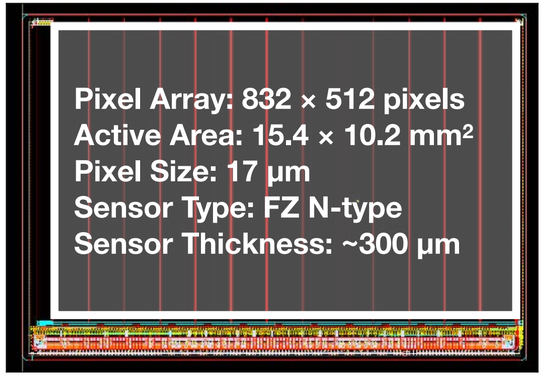


Telescope

KEK AR Test Beam Line (AR-TB): Electron beam (1- 4 GeV)

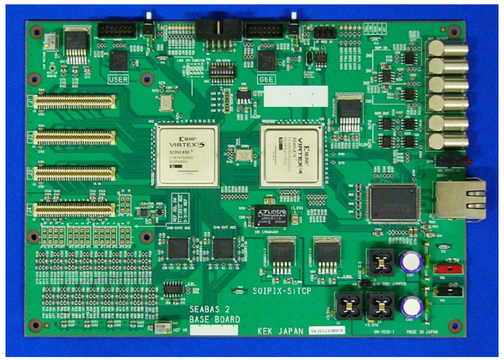


INTPIX4



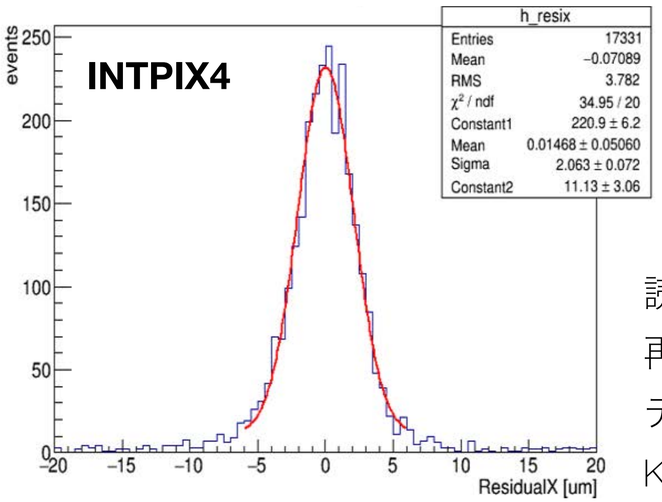
Analog signal readout
(13 block parallel)

DAQ Board (SEABAS2)



Readout:
12 bit, 16 ch ADC

Residual

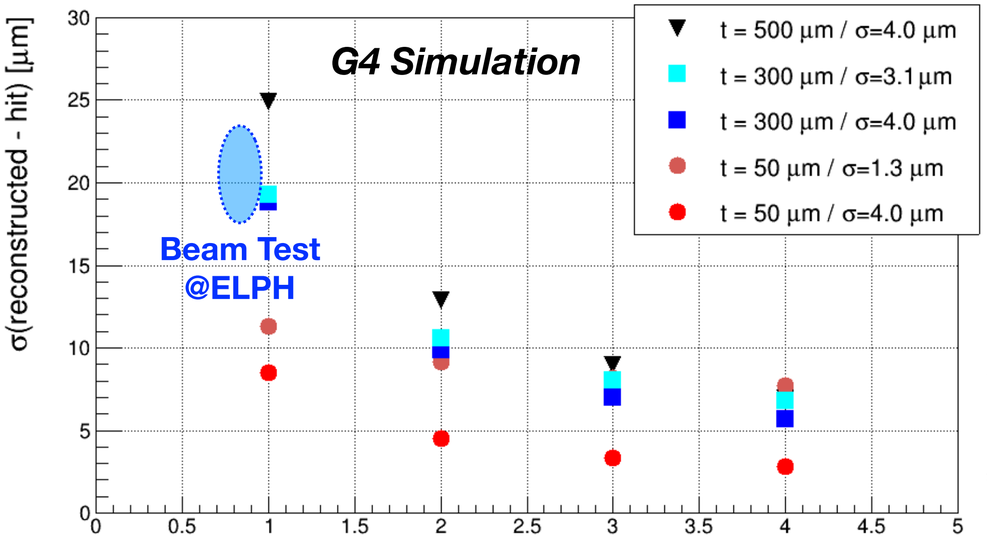


筑波大学，素粒子実験研究室
山内大輝，修士論文，2019 年

Position resolution: 1.56 µm @FTBL in 2019

読み出し速度向上のために
再設計を行なった **INTPIX4NA** により
テレスコープシステムを構築する.
KEK AR-TB での実用化を目指している.

ビームエネルギーに対する位置分解能のシミュレーション



筑波大学
素粒子実験研究室
鈴木尚紀

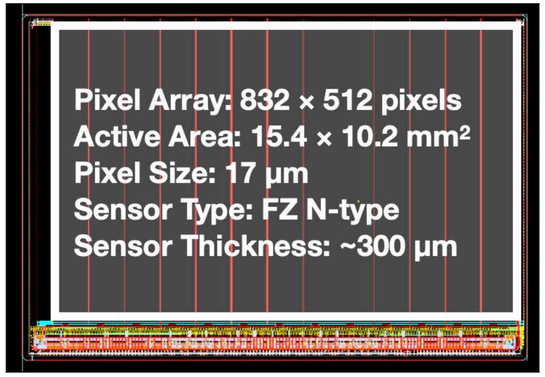
物理学会，2021 年

ADC 分解能の見積もり

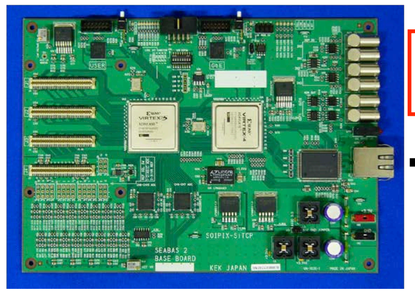
位置分解能を維持しつつ，読み出し速度向上のために必要な ADC の分解能を見積もる.

ビームエネルギー 4 GeV のとき，INTPIX4 の有感領域におけるビームレートはおよそ

100 — 300 Hz 程度.



13 → アナログ信号読み出し
（13 ブロック並列）



SEABAS2
FPGA 搭載 DAQ ボード

Readout:
12 bit, 16 ch ADC

→ PC へ送信

位置分解能
電荷重心法で精度良くヒット位置が再構成可能な ADC のビット数

↕ トレードオフ

読み出し速度
ビームレートと同程度のレートで有感領域全体を読み出せる ADC のビット数

↓

実ビームを使ってヒット位置の再構成とトラック再構成，
位置分解能への影響を評価する.

必要統計量とビームタイムの見積もり

Frame rate: 35 Hz @ ADC 12 bit（2016 年のデータより）

1 Run: 30,000 events/30 min（10 s/1 spill, 14 s interval）

↓ Tracking Efficiency ~10%

1 Run: 3,000 tracks/30 min
4 bias points × 12,000 tracks = 4 × 4 × 0.5 h = 8 h
3 sensors × 8 h = 24 h (2 shifts)

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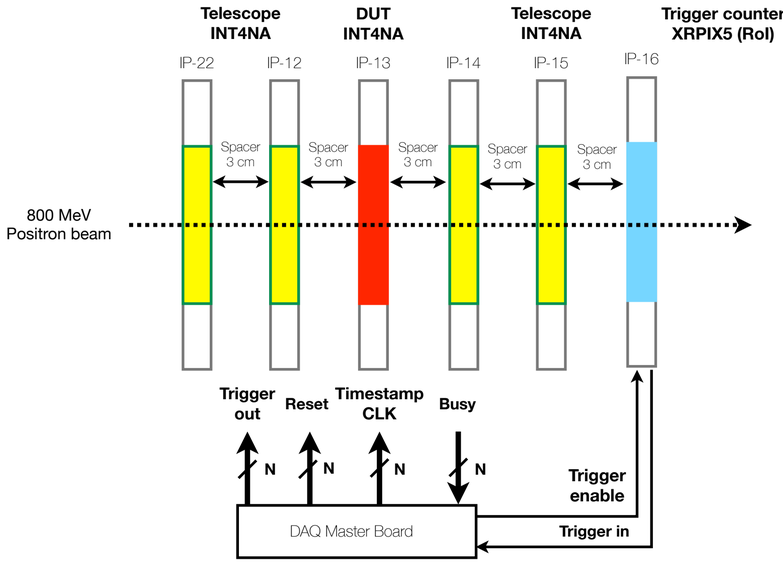
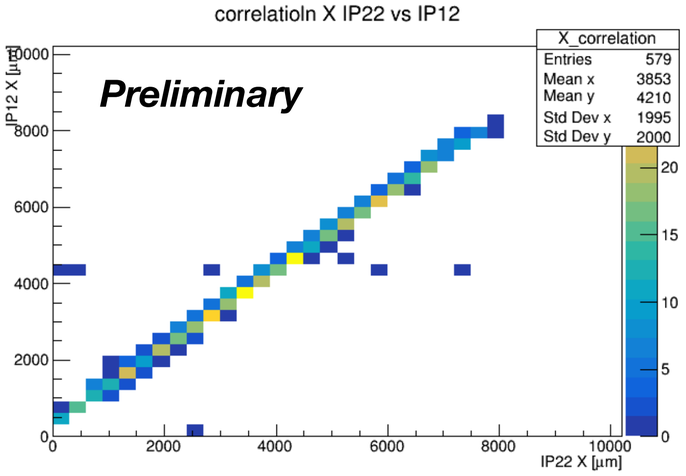
Telescope

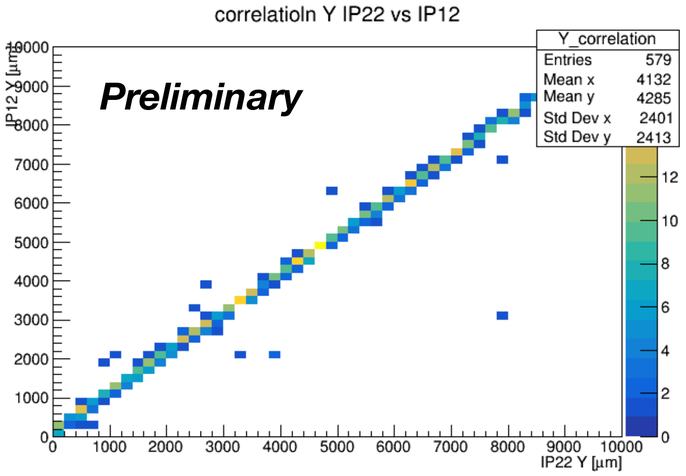
Beam Test @ELPH (800 MeV Positron Beam)



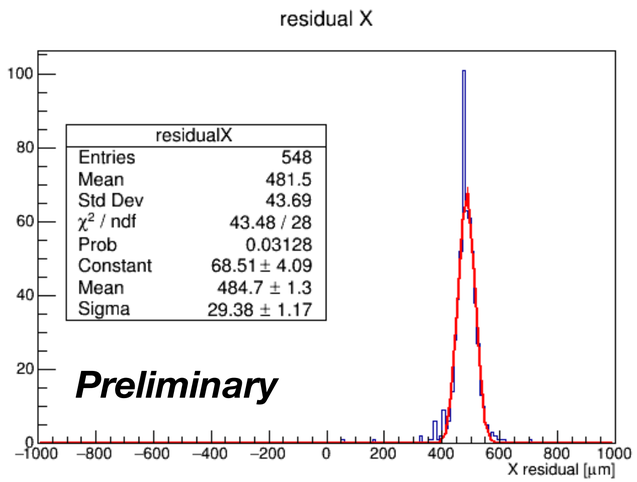
筑波大，宮崎大，都立産技高専

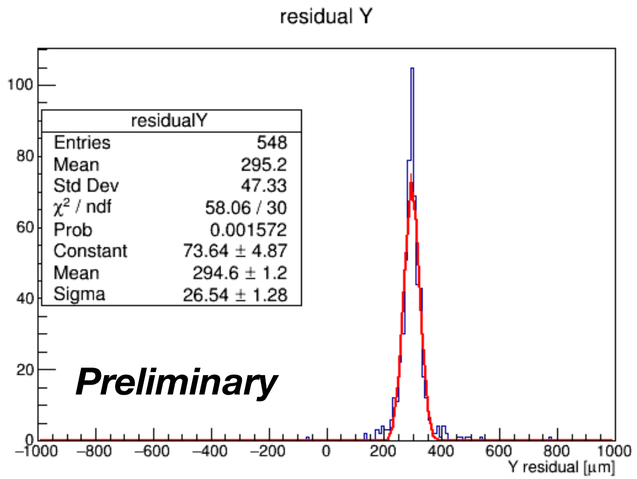
Hit Position Correlation





Residual





現地での解析結果速報

位置分解能: 30-26 µm（センサー間アライメントなし）

参考: G4 Simulation ~25 µm（800 MeV e^+, 300 µm 厚センサー）

Summary

SOI 技術によるセンサー部回路部一体型のモノリシック型ピクセル検出器の開発を行なっている.

特に ILC 実験での崩壊点検出器での実用化を目指しプロトタイプ SOFIST の設計，評価を行なってきた.

SOFIST

全ての必要な機能をピクセル内に実装した SOFIST4 の評価を進めている.

- 金マイクロバンプを用いた三次元積層化技術により，ピクセルサイズを 20 μm に保ちつつ，
  回路実装面積の拡張に成功した.
- マイクロバンプ接続歩留まりは 99.9 % を確認している.
- ビーム試験により，ヒットの検出を確認している．現在はトラックの再構成と詳細アライメントを進めている.
- 今後の課題は消費電力と放射線耐性である．消費電力削減のため，ピクセル部のアナログ回路を再検討する必要がある.

Telescope

センサー性能評価用のテレスコープシステムの開発も行っている.

KEK AR-TB での実用化を目指し，システムの構築，性能評価を行っている.

- ビーム試験データの解析を進めている．現地の解析にて位置分解能についてはシミュレーションに近い値を得ている.
- 今後の課題はビームレートに合わせた DAQ レート（読み出し速度）の向上である.